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biomation

MODEL K100-D/32
INPUT ADAPTER

OPERATING AND SERVICE MANUAL

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GOULD
An Electrical/Electronics Company

The above photograph shows the K100-D/32 Input Adapter in use on and Intel SDK 8086 board.

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NOTICE

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SECTION I

GENERAL INFORMATION

1.1 Certification

Gould Inc. certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory.

1.2 Warranty

All Gould Inc. products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products that prove to be defective during the warranty period. If a unit fails within thirty days of delivery, Gould Inc. will pay for all shipping charges related to the repair of the unit. Units under warranty, but beyond the thirty day period, should be sent to Gould Inc. prepaid and Gould Inc. will return the unit prepaid. Units out of the one year warranty period, the customer will pay all freight charges. IN THE EVENT OF A BREACH OF GOULD INC.'s WARRANTY, GOULD INC. SHALL HAVE THE RIGHT IN ITS DISCRETION EITHER TO REPLACE OR REPAIR THE DEFECTIVE GOODS OR TO REFUND THE PORTION OF THE PURCHASE PRICE APPLICABLE THERETO. THERE SHALL BE NO OTHER REMEDY FOR BREACH OF THE WARRANTY. IN NO EVENT SHALL GOULD INC. BE LIABLE FOR COST OF PROCESSING, LOST PROFITS, INJURY TO GOODWILL, OR ANY SPECIAL OR CONSEQUENTIAL DAMAGES. THE FOREGOING WARRANTY IS EXCLUSIVE OF ALL OTHER WARRANTIES, WHETHER EXPRESSED OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OF FITNESS FOR A PARTICULAR PURPOSE.

1.3 Description

The Model K100-D/32 Input Adapter (see Figure 1.1) transforms the Model K100-D Logic Analyzer from a 16-channel timing and data domain instrument into a 32-channel data-domain-only instrument. In addition to the extra channels provided by the adapter, it also provides user selectable circuitry necessary for extensive OR clocking and demultiplexing capabilities to match the needs of the most advanced microcomputers.

Figure 1.1 The Model K100-D/32 Input Adapter comes complete with a flying lead ribbon cable and a 40-pin DIP clip. The input cables to the K100-D and the power cable are also included.

The accessory connects directly to the K100-D front panel inputs. The K100-D automatically senses the presence of the adapter, and executes a branch to the appropriate firmware subroutines for 32-channel operation. Both the video display and the keyboard operation of the K100-D change to reflect the new record parameter options available in this mode. These changes include: (1) reconfiguration of the data memory from 1024 16-bit words into 512 32-bit words; (2) using the Enable field as the 16-bit fixed sequence address portion of the trigger word; (3) using the Trigger field as the 16-bit variable sequence data portion of the trigger word; and (4) extending the search mode to 32 bits.

1.4 Model K100-D/40 Input Adapter

This accessory was especially designed to provide a flexible signal conditioning enclosure for use with the Model K100-D/32 Input Adapter. You can simplify system connection and eliminate the need for individual probe leads by wire wrapping the test signal connections inside the enclosure. Also, the accessory has space for adding active pre-processing circuitry and gives direct access to all test signals to facilitate parallel testing. See Figures 1.2 and 1.3.

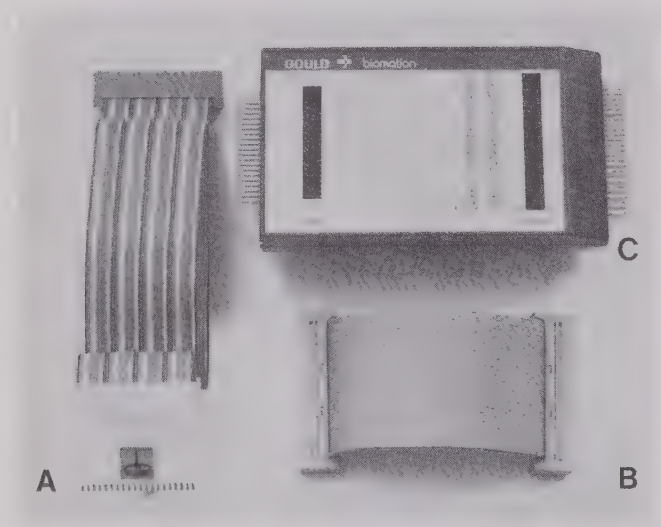

Figure 1.2. Each Model K100-D/40 Input Adapter is shipped complete with A) and 18 inch input cable with DIP clip; B) a 3 inch output cable that connects the K100-D/32 (32-channel adapter); and C) a K100-D/40 PC board and enclosure assembly.

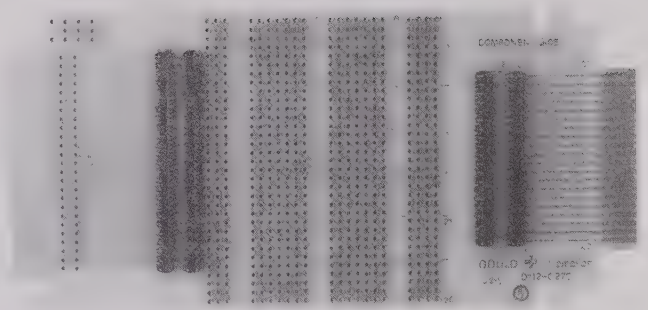

Figure 1.3 The K100-D/40 PC board is shown above with the enclosure removed. Standard-sized 0.635 mm (0.025 inch) wire wrap square posts are provided for monitoring all input (40) and output (50) pins. (Shown approximately 45% of actual size.)

In addition, the clock options are restricted to external clock only and the maximum external clocking rate is reduced from 70 to 12 MHz. Similarly, the maximum selectable trigger delay of either clock intervals or trigger events is reduced from 65,530 to 32,765 and the Trigger Out signal from the rear panel of the K100-D is not usable in this mode. Threshold levels are fixed at TTL only. Power for the adapter is provided by connecting its attached LEMO-type receptacle cable to either one of the two matching power jacks located on the rear panel of the Model K100-D Logic Analyzer.

1.5 Specifications

SIGNAL INPUTS

Number. 36, including 16 address, and 16 data, plus 1 clock, and 3 qualifiers. Entire address field logic selectable positive or negative polarity. Data field logic selectable on a bit-by-bit basis.

Load. Data and qualifier inputs $I_{IL\ max}$ = 0.2 mA TTL level.

Threshold. Fixed TTL.

Maximum Voltage. +5.5 V, -0.5 V.

Mechanical Connection. Via 50-pin multiconductor ribbon cable that terminates to labeled individual connectors. These connectors mate to 0.025 inch square posts found on the supplied 40-pin IC spring clip, or on any standard wire wrap posts.

CLOCK

External input only. Via the K100-D/32's multi-conductor ribbon cable.

Load. $I_{IL\ max}$ = 0.8 mA TTL levels.

Threshold. Fixed TTL.

Rates. DC to 12 MHz.

Pulse Width. 30 ns minimum.

Slope. Active-edge selectable, rising or falling.

Set-up and Hold Time. 20 ns and 0 ns maximum, to the active edge chosen.

Clock Qualifiers. Three dedicated clock qualifiers. CKB, CKC, and CKD are available via the multiconductor input ribbon cable. These qualifiers allow a variety of OR clocking options through internal strapping. CKB and CKC are active high. CKD is active low.

TRIGGER

The K100-D/32 has a single 32-bit combinational trigger word divided into two 16-bit fields; one field for address and one for data. The address field is defined by the Enable word in the status mode of the K100-D, while the data field is defined by the Trigger word.

Sources. Manual or combinational.

Manual--Via front panel trigger switch.

Combinational--The unit is triggered when the input data matches the selected combinational states of both the address and data portions of the trigger word.

Arm. Selectable Manual--Via the front panel Arm switch. Auto--Auto Stop, or Auto Stop with limits.

DISPLAY

There are two display modes for 32-channel operation, Status and Data.

Status. The K100-D automatically detects the presence of the adapter and calls up a unique display. This display is similar to that used in normal operation, but shows only the options available for the 32-channel recordings.

There are three separate status displays (W, A, and B). Each display shows all the conditions specified for the next, current, and reference recordings.

Data. Memory contains 512 32-bit words. Each word is displayed as a two line entry. The first line shows the address, which has a nonalterable sequence and grouping. The second line shows the data, which is fully user selectable for both sequence and grouping. Data can be viewed in either hexadecimal, octal, binary or ASCII characters.

MISCELLANEOUS

Size. 9.2 cm (3.6 in.) wide; 17.3 cm (6.8 in.) deep; 2.5 cm (1 in.) thick.

Weight. 0.5 kg (1 lb.).

Power. +5 V at 1.1 A maximum, -5.2 V at 0.3 A maximum. Power obtained from either of the two rear panel LEMO connectors on the K100-D.

Accessories Included. Unit is supplied with a 40-pin IC spring clip, flat ribbon input and output cables, captive power cord, and a copy of the Operating and Service Manual. The firmware required for operation is already resident in the Model K100-D Logic Analyzer.

Item*	Biomation Stock No.
Spare Data Input Cable	0112-0149
Spare 40-pin IC Spring Clip	6000-0248
Extra Operating and Service Manual	0112-0159

*Consult factory for current prices.

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SECTION II

INSTALLATION

2.1 Introduction

This section contains information on the unpacking, inspection, storage, shipment and power connection of the Model K100-D/32 Input Adapter.

2.2 Unpacking and Inspection

Inspect the adapter for shipping damages as soon as it is unpacked. Check for broken wires and loose connectors. Inspect the case for dents and scratches. If the adapter is damaged in any way, or fails to operate properly, notify the carrier immediately. For assistance of any kind, including help with instruments under warranty, contact your local representative or the Gould Inc., Instruments Division, Biomation Operation, factory.

2.3 Storage and Shipment

Should it become necessary to store or ship your adapter, always remember to protect it as well as possible to prevent damage from extreme environmental conditions or abusive handling. To protect this, or any valuable electronic equipment during shipment, always use the best packaging methods available. Contract packaging companies in many cities can provide dependable custom packaging on short notice.

2.4 Power Connection

The Model K100-D/32 Input Adapter requires ± 5 VDC for operation. This power is supplied from two marked, LEMO-type jacks located on the rear panel of the K100-D.

2.5 Preparation for Use

The Model K100-D/32 Input Adapter is set up for normal 32-channel operation and is ready for immediate use. All that is required is to connect the input leads to the system to be tested, plug the output cables into the K100-D front panel, and to plug the power jack into the rear panel. Special test situations, however, can be handled much more easily by using the clocking and demultiplexing capabilities available via internal strapping (see Section 3.4 for details).

2.6 Initial Warm-up

The Model K100-D/32 Input Adapter is a solid-state instrument. It has been thoroughly burned-in and tested at the factory. No special warm-up period is required before use.

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SECTION III

OPERATION

3.1 Introduction

This section explains the use and function of the signal inputs, as well as the front panel operation and displays, of the Model K100-D Logic Analyzer when used with the 32-channel adapter. Although 32-channel operation is similar in overall philosophy to the K100-D's normal 16-channel mode, some parameter choices are extended, while others are restricted and all of the internal timing functions have been eliminated. No attempt is made to explain 16-channel operation in this manual. Interested readers should refer to the standard K100-D Operating and Service Manual.

3.2 Signal Inputs to the Adapter

All signals from the System Under Test (SUT) are fed to the 32-channel adapter via the marked, flying lead connectors of the standard data input cable accessory. These flying lead connectors attach directly to the DIP clip included with your adapter, to the hook-type grabbers that were included with your K100-D, or to any standard size (0.025 inch or 635 mm) wire wrap pins.

Table 3.1 (see next page) has been provided as a convenient guide to the pin assignment of these signals, and as a brief description of their assigned functions in normal operation. Note, however, that all 32 signals marked as address and data are dedicated only as a convenience to facilitate ease of connection and the subsequent interpretation of recording results. If your test situation requires, these signals can be individually assigned to suit your needs. Because of the adapter's bit-level triggering specifications, and the K100-D's flexible formatting capabilities, you can use the instrument as a general purpose 32-channel data recorder on any synchronous TTL logic system simply by viewing all resultant data displays in the most convenient, applicable format (Hex, Octal, Binary, or ASCII).

3.3 Front Panel Operation and Displays

3.3.1 Front Panel Control Alterations

The functioning of several keys and switches on the K100-D front panel are altered in the 32-channel mode to reflect the new parameter options for both recording and data display. One switch, the Auto/Manual Enable, has been functionally eliminated, along with three keys, Threshold, Input and Timing. The functioning of one other switch, the Filtered/Manual Trigger, is restricted to manual trigger only. The functioning of 17 other multi-function keys has been reduced to reflect only the choices available for TTL data domain analysis.

The K100-D's high self-teaching ability and automatic error detection features greatly simplify the task of familiarizing yourself with 32-channel operation. Any attempts to enter meaningless or inoperable keystrokes causes the error light to turn on so that you know instantly when you have tried to execute an undefined sequence.

3.3.2 Status Displays

Operating in the 32-channel mode, the K100-D retains the same three status displays as in the 16-channel mode, W, A, and B. "W" is the working, or next recording, display. "A" displays the parameters (recording conditions) used for the last recording made, and "B" displays the parameters of the recording held in the reference memory. When first turned on, the instrument does complete self-diagnostics of all ROM, RAM, and keyboard functions. It then defaults to the 32-channel Status A display with Power Up Complete appearing in the upper left hand corner of the CRT if the tests are passed. These default conditions are shown in Figure 3.1.

Note that all the fields shown in reverse video can be altered directly via the keyboard.

Table 3.1 Data Input Cable Pin Assignments

Corresponding Channel in Display Sequence	Pin Number	Sleeve Marking	Sleeve Color	Signal
1. Data 0	1	D0	Yellow	Lower Data Byte (Least Significant Bit)
2. 1	2	D1		
3. 2	3	D2		
4. 3	4	D3		
5. 4	5	D4		
6. 5	6	D5		
7. 6	7	D6		
8. Data 7	8	D7	Yellow	Lower Data Byte (Most Significant Bit)
	9	None	Black	Lower Data Byte Ground.
9. Address 0	10	A0	White	Lower Address Byte (Least Significant Bit)
10. 1	11	A1		
11. 2	12	A2		
12. 3	13	A3		
13. 4	14	A4		
14. 5	15	A5		
15. 6	16	A6		
16. Address 7	17	A7	White	Lower Address Byte (Most Significant Bit)
	18	None	Black	Lower Address Byte Ground.
17. Address 8	19	A8	Yellow	Upper Address Byte (Least Significant Bit)
18. 9	20	A9		
19. A	21	A10		
20. B	22	A11		
21. C	23	A12		
22. D	24	A13		
23. E	25	A14		
24. Address F	26	A15	Yellow	Upper Address Byte (Most Significant Bit)
	27	None	Black	Upper Address Byte Ground.
25. Data 8	28	D8	Yellow	Upper Data Byte (Least Significant bit)
26. 9	29	D9		
27. A	30	D10		
28. B	31	D11		
29. C	32	D12		
30. D	33	D13		
31. E	34	D14		
32. Data F	35	D15	Yellow	Upper Data Byte (Most Significant Bit)
	36	None	Black	Upper Data Byte Ground.
	41	ALE	Blue	Address Latch Enable. Not Recorded.
	42	None	Black	Address Latch Enable Ground.
	43	CKA	Red	Clock Qualifier A. Not Recorded, Active High.
	44	CKB		Clock Qualifier B. Not Recorded, Active High.
	45	CKC		Clock Qualifier C. Not Recorded, Active High.
	46	CKD*	Red	Clock Qualfier D. Not Recorded, Active Low.
	47	None	Black	Clock Ground. This ground should always be connected to the SUT. In most cases, the other grounds need not be connected unless improper operation occurs.
	48	None	Black	Spare Clock Ground.

*Since CKD is active low, it **must** be grounded if not used.

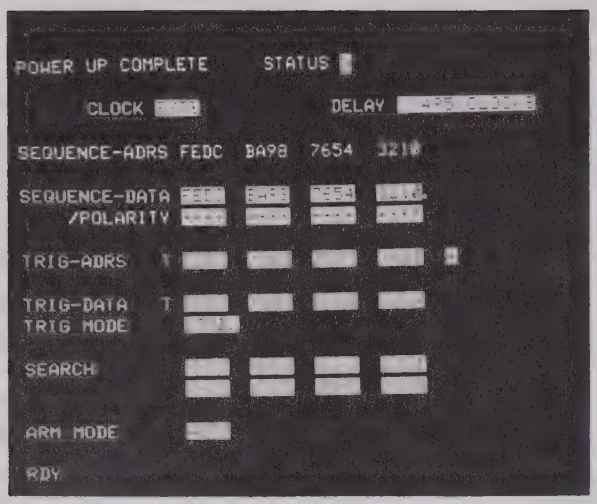


Figure 3.1 Power up Status display showing default conditions.

Addressing any of these fields causes the Status A display to transfer to the Status W display, and the cursor to move to the field addressed. To recall the original Status A display, push the blue button A. To recall the reference Status B display, push the blue button B.

3.3.3 Recording Parameters

Clock

You can select either the external rising or the external falling edge of the clock. Since only synchronous recordings are applicable, no internal clock options are available. The recording clock is formed by a combination of four clocks, Clock A (CKA), Clock B (CKB), Clock C (CKC), and Clock D (CKD).

CKA acts as the master clock and is qualified by CKB, CKC and CKD. CKA, CKB, and CKC are active high, while CKD is active low. Since all four clocks are TTL signals, they tend to float high, so CKD must be grounded if unused. To be assured of proper operation, you should also hold CKB and CKC high if they are not needed for a particular recording, thus avoiding any possibility of their being pulled low through unwanted crosstalk.

In normal operation all four clocks are ANDed together so that CKS, CKB, and CKC must be high and CKS low to receive a clock pulse out from the adapter to the K100-D. Since CKA is the master clock input, it is the signal for which the clock edge is selected.

Delay

Either Delay by Clocks or by Events may be selected simply by pressing the rightmost switch below the CRT to match your choice. If Delay by Clocks is used, the delay entered will equal the number of clocks following the recognition of the trigger event to memory location 500. For example, even though the memory length in 32-channel operation is 512 words, entering a delay of 500 clocks will cause the trigger event to appear at memory location 000, not 012. Similarly, using the default delay of 495 clocks result in the trigger event being positioned at memory location 005. The clock delay range is keyboard selectable from 0 to 32,765 clocks.

If Delay by Event is selected, the event referred to is the occurrence of the specified 32-bit combinational trigger word. The Nth+1 occurrence of this trigger word (where N equals the number of event delays selected) will always appear at memory location 250. The event delay range is also keyboard selectable from 0 to 32,765 events.

Sequence

Referring to Figure 3.1, note that there are two separate Sequence fields, one marked Address and one marked Data/Polarity. The sequence of the address field is fixed, as noted by its nonreversed video display, and is shown for convenience only. The sequence of the data field, however, is completely selectable, both in terms of order and grouping size. As in 16-channel operation, data displayed in the special mode is decoded into ASCII characters if grouped into seven channels. Data is further decoded in Hexadecimal if grouped into four, Octal if grouped into three, or Binary if alone. The polarity of the data field is also channel selectable, and can be altered by moving the cursor to the channel of interest, pressing the black plus or minus key as desired, then pressing the Enter key.

Trigger

Corresponding to the sequence fields, the 32-channel trigger is also divided into address and data fields. The address portion is opened by pressing the Enable button, while the data portion is opened by depressing the Trigger button. The nonreverse video T just to the left of each field is there to indicate that only true triggering (i.e., triggering on the actual occurrence of the combinational fields) is available.

NOTE: The 32-channel trigger comes true on state rather than edge transitioning as is the case in 16-channel operation. Therefore all that is required for a trigger to be recognized is that the bit combination selected be true when sampled by the external clock.

The reverse video plus sign to the right of the trigger Address field indicates the selected polarity of the entire 16-bit field. This polarity can be changed by opening the Trigger Address field, moving the cursor underneath the sign and changing it as desired. The trigger word, both address and data portions, can be entered in either hexadecimal (using the white keys) or binary 1's, 0's, and don't cares (using the black keys).

CAUTION: THE NORMAL TRIGGER MODE IS COMBINATIONAL. HOWEVER, MANUAL OVERRIDE CAN BE USED SIMPLY BY DEPRESSING THE MANUAL TRIGGER SWITCH LOCATED BENEATH THE DISPLAY. THIS WILL CAUSE WHATEVER DATA VALUE THAT HAPPENS TO BE PRESENT AT THAT TIME TO BE ACCEPTED AS THE TRIGGER AND WILL IMMEDIATELY INITIATE THE DELAY COUNT TO THE END OF THE RECORDING. BECAUSE OF THE WAY THE ADAPTER INTERFACES TO THE K100-D, THE RESULTING RECORDING WILL VERY LIKELY SHOW THE ADDRESS AND DATA FIELDS REVERSED SO THAT ACTIVITY ON THE ADDRESS CHANNELS APP ON THE DATA CHANNELS AND THE DATA CHANNELS APPEARS ON THE ADDRESS CHANNELS. FOR THIS REASON, BE SURE TO CAREFULLY REVIEW ALL RECORDINGS MADE USING THE MANUAL TRIGGER FOR PROPER DATA FIELD ORIENTATION.

Search

This parameter field operates on the data domain display but does not effect recordings. When in Status display mode, it can be opened by using the blue Search key. You can specify in binary or hexadecimal any bit combination or word up to the full 32-bit width that you wish to find in the data domain display of a recording. Once a combinational search word has been entered, the K100-D automatically searches for that word in memory.

The Search mode allows you to spotlight any particular sequence in a loop, or data progression, so that you can study the structure of actual program behavior surrounding the combinational occurrences of interest. Note that only the relevant channels should be entered in the search mode while the others should be left in the Don't Care (X) positions. This gives you the flexibility of highlighting in memory only those states that you wish to locate.

Example: Using the data automatically stored in memory upon power up, you can use this mode to search for the hexadecimal letter A, formed by combining Data channels 8, 7, 6 and 5. This example illustrates the functioning of both the Search and Sequence fields. In the Status display, first open the Data Sequence display by pressing the Sequence key. Reenter channels F through 9 consecutively, and press the space key. Enter channels 8 through 5, and press the space key. Enter channels 4 through 2 and press the space key. Enter channel 1, and press the space key. Enter channel 0, and press the space key, period, space, and Enter. Second, open the Search field and advance the cursor until it is underneath channel 0 at the far right of the first, or address, row. Key in an X and move the cursor on down into the second row beneath channel 8. Key in a hexadecimal A, and press enter.

The Status display should now look like Figure 3.2.

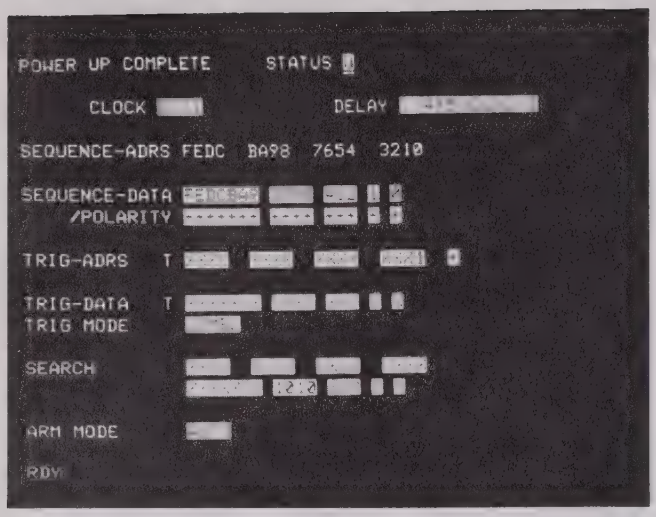


Figure 3.2 Status display with altered sequence and Search fields.

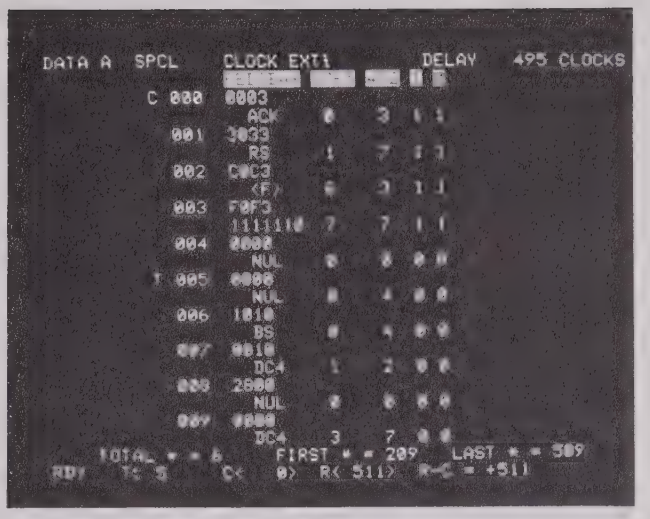


Figure 3.3 Display with Data, Special, and Search keys depressed.

Press the blue Data Key, the white Special key, and the blue Search key. Your display will look like Figure 3.3.

Note that all 16-channels of the address are in Hexadecimal, while the data channels underneath are shown respectively in ASCII, Hex, Octal and Binary groupings. The message on the second line from the bottom of the display informs us that there were six occurrences of the Combinational Search word found in memory. The first is located at 209, and the last is at 509.

All six occurrences are marked by an asterisk just to the right of their memory location. To view the first occurrence, press Specify, press either key of the C cursor, key in 209, and press Enter. The data display will automatically advance to location 209, as in Figure 3.4, so that you can view the first occurrence of the search word.

Figure 3.4 Data display after advancing to location 209.

Arm Mode

You can select either Auto or Manual Arm simply by pressing the Auto/Manual Arm switch beneath the display, just as in 16-channel operation. Auto Stop on A=B, A≠B, or with limits is also available. When limits are used, the unit compares only the data between cursors and on the channels displayed. Since the address channels cannot be removed from the data display, the minimum limits comparison in the 32-channel mode is 16 bits of address, and 1-bit from the data when all but one of the data channels have been removed and the two cursors are at the same location.

3.3.4 Status Bytes

There are five different status bytes, RDY, CK?, TG?, DLY, and BSY to help monitor a recording in progress. One of these status bytes is visible at all times in the lower left-hand corner of both the status and the data displays. Below is a tabulation of the meaning of both of these bytes in the order in which they are displayed.

RDY

The unit is ready for an Arm event to make a new recording. The only time you see this display is when you are in the Manual Arm mode. If you have armed the instrument, and wish to get it back into a Ready-for-Arm status, press the Manual Arm switch down a second time. This cancels, or aborts, the current recording in progress.

CK?

When the clock is not active or is extremely slow in your system, or the clock qualifier conditions are not met, the instrument responds by asking for a clock. This occurs only when trigger holdoff is operational.

TG?

The unit is waiting for the trigger event. It accepts either the selected 32-bit combinational trigger word or you can press the Manual Trigger switch. (Refer to the CAUTION notice contained in the last paragraph of the Trigger parameter discussion.)

DLY

The unit is counting down trigger delays, either in terms of clock periods or trigger events. When DLY is no longer displayed, it means that the recording has been completed, and the following message may appear:

BSY

The unit has completed the measurement and is now updating the display memory. It does not record any information during this

period of time. When it has finished, it automatically updates the data display to show the new recording. Assuming a Manual Arm, the status byte will then revert to RDY, indicating that the recording has been completed. The instrument is ready to be armed again at your convenience.

3.3.5 Data Displays

There are four basic types of data displays, Hex, Octal, Binary, and Special. Any of these displays can be entered from the Data mode simply by pressing the corresponding white key to the left of the blue Data key. Pressing the Binary, Octal, or Hex key forces the channels into appropriate groupings for these modes. The Special mode, which was demonstrated earlier in the example contained in the Search section, decodes the data in accordance with the size of the groups which are specified by the sequence field. Since the sequence of the 16-channel address field is fixed into four four-channel groupings, use of the Special Mode always decodes these channels into four hex characters.

The 16-channels of the data field, which were arranged into groups of 7, 4, 3, and 2 individual channels, are decoded into ASCII, Hex, Octal and Binary respectively. If you followed the earlier search example, then your instrument should show the Special Mode data display in Figure 3.4. Typical examples of the other three formats can be obtained by pressing the Hex key (Figure 3.5), the Octal key (Figure 3.6), and the Binary key (Figure 3.7). The data shown by all four displays is identical, but reformatted for your convenience in viewing so that you an select the most applicable display for a particular recording.

To view other portions of a recording, you can either use the C cursor directly to step forward and backward through the recording, or go straight to a particular portion by specifying that position. To specify a particular position, press the blue key, Specify, and either of the C cursor buttons. The C cursor field at the bottom of the display changes to reverse video. Key in the location desired, press Enter, and the display will automatically move to the new location.

To delete, add, or rearrange the 16 Data channels on the display, simply open the Sequence field, make the desired changes just as in the Status mode, and press Enter. Note that this is only a display function so that the data held in memory is still present for convenient recall whether or not it is currently displayed.

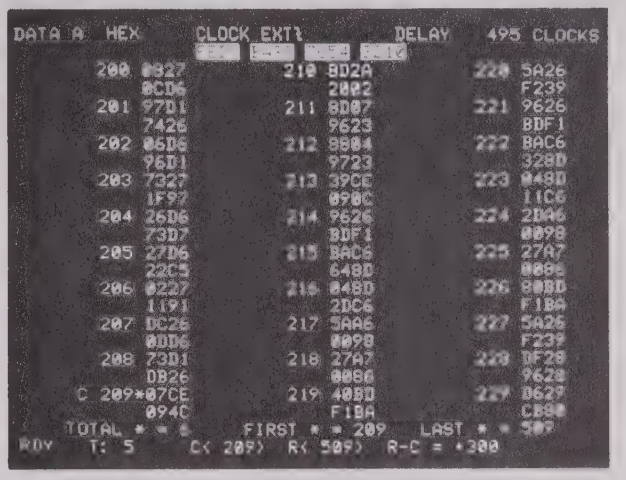


Figure 3.5 Data display in Hex.

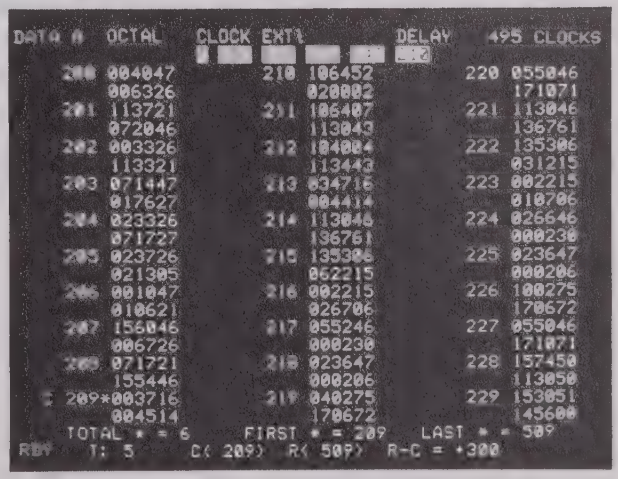


Figure 3.6 Data display in Octal.

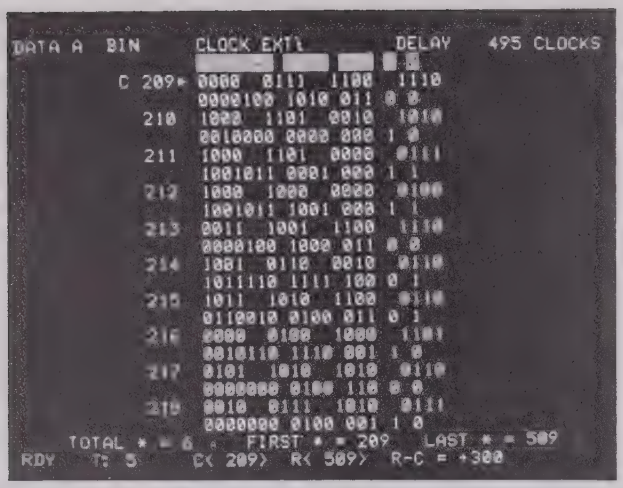


Figure 3.7 Data display in Binary.

3.4 Using Your Adapter With Popular Microprocessors: Alterations for OR Clocking and Demultiplexing

3.4.1 Introduction

This section describes how to modify the adapter so that recording program executions from a number of specific microprocessors is easier and more efficient. Also, connection of the adapter to a number of microprocessors is discussed briefly to give you some examples of the adapter's use. There are four different 32-channel adapter configurations (10, 20, 30, and 40) that you can choose from depending on which microprocessors you are testing. Version 10 is the standard configuration while Versions 20, 30 and 40 represent restrapped modifications you can make yourself. These four versions handle most 40-pin IC package microprocessors, both 8 and 16-bit types.

Version 10 refers to the standard adapter as shipped from the factory. As discussed in section 3.3.3, the four clock signals (CKS, CKB, CKC, and CKD) are ANDed together. CKA is the master clock input and its edge (polarity) is selectable from the keyboard. Using an asterisk (*) to describe active low signals, the Boolean expression of this relationship could be written as CK=(CKA CKB CKC CKD*) when the leading edge ( ) of CKA is selected. The microprocessors for which this version is suitable include the 6800, 6802, 6809, and 6502.

Version 20 modifies the clock circuitry for OR clocking. The new Boolean expression resulting from this modification is CK=(CKA+CKB+CKC+CKD*). The edge of CKA is no longer keyboard selectable but can be changed by moving a jumper (M3) to obtain CK=CKA*+CKB+CKC+CKD*). The microprocessors for which this version is suitable include the 8080, 8088, and 8086.

Version 30 changes the routing of the address and data latches to demultiplex the 8085 microprocessor. The clocks are ORed just as in version 20.

Version 40 is a special version of OR clocking required for use with microprocessors having one or several control (i.e., clock) signals that are valid only for very short time periods (less than 20 ns) such as the Z80A and the Z8002. Briefly, the microprocessor's system clock is fed into CKA causing fresh data to be stored in the latches on every cycle of the system clock. That data, however, is only transferred to the logic analyzer's memory when one of the other clocks (CKB, CKC, or CKD) becomes true. The edge of CKA remains keyboard selectable and the resulting Boolean expression is CK*=(CKB*+CKC*+CKD). This version requires nonstandard jumping which will be treated separately in Section 3.4.3.

CAUTION: BEFORE ATTEMPTING MODIFICATION OF YOUR ADAPTER, DISCONNECT ALL CABLES FROM THE K100-D TO PREVENT POSSIBLE ELECTRICAL SHOCK OR CIRCUIT DAMAGE. THEN REMOVE THE CASE, BOTH HALVES OF WHICH ARE SECURED BY FOUR PHILLIPS HEAD SCREWS LOCATED ON THE ADAPTER'S BOTTOM SIDE. WHEN THE MODIFICATIONS ARE COMPLETE, REASSEMBLE THE ADAPTER. TO PREVENT POSSIBLE CONFUSION, BE SURE TO MARK WHICH VERSION APPLIES IN A PROMINENT POSITION ON THE ADAPTER'S LABEL.

3.4.2 Modifications for Versions 10, 20, and 30

Table 3.2 describes the jumper positioning for the first three versions, lists specific microprocessors appropriate to each version, and notes the proper orientation fo the jumpers to match the table. There are five primary jumpers and eight secondary jumpers. The five primary jumpers (M1-M5) can be changed from version 10 by cutting the existing traces and adding new wire jumpers. The positions of M1 and M2 determine the polarity of CKA when the clocks are ORed. M4 and M5 ties in the ALE signal to demultiplex the 8085. The eight secondary jumpers are used only for version 30 and complete the demultiplexing of the 8085.

Figure 3.8 shows the physical locations of all the jumper areas indicated in Table 3.2 from the component side of the adapter board. Each jumper area is circled and labeled to match Table 3.2 and the jumper locations, row, and column markings are etched onto the board's surface. **The cutting of existing traces and soldering of new jumpers must,** of course, **be done from the opposite,** or **solder side of the board, which is shown in Figure 3.9.** Again the jumper areas are circled and labeled to match Table 3.2. **Since this is the side** that you'll be working with, it is also the side **that the jumper positions are referenced for (Up, Down, Right, or Left) in the table.** Figure 3.8, the top view, is included only to add clarity and help you locate the jumper positions. Similarly, Figure 3.10, which shows the jumper areas as they appear on the schematic of the 32-channel adapter, is included so that you can understand the effects of the various modifications.

3.4.3 Modifications for Version 40

Version 40 is a special, nonstandard modification of the adapter (as mentioned in Section 3.4.1) that facilitates efficient recording of Z80A and Z8002 activity. The actual modifications needed to change the adapter are fairly limited, as you can see by referring to Figure 3.11 which shows the necessary schematic changes to the adapter. Physically, these changes amount to six cuts shown in Figure 3.12) and four jumpers (all on the solder side of the board as shown in Figure 3.13).

NOTE: Since the changes are not referenced to designated jumper areas you should use extra care to avoid damaging the board. Also, be aware that while the board can be changed back again by reversing the cuts and jumpers, this should be avoided if possible, again to avoid accidental damages to the board.

3.4.4 Recommended Signal Connectors

Table 3.3 is a recommended guide for connecting the flying leads of the adapter to specific microprocessors. The connections are as comprehensive as possible. Much more selective recordings can be made using only single clock signals or by clocking from different combinations of status signals and control lines. When you've familiarized yourself with the adapter's operation on a particular system, you'll find that several slightly different signal connections can be used depending on the recording desired. The best way to determine the proper connections for a particular test is by studying that microprocessor's signal definitions and timing sequences to determine when the signals you want to record are valid. This information can be obtained directly from the microprocessor manufacturer or by consulting reference guides such as Osborne and Associates' "An Introduction to Microprocessors," Volume 2.

For additional convenience and flexibility in handling microprocessors and other specialized logic systems, the Model K100-D/40 Input Adapter is available. See Accessories Available in Section 1.4 for information on this accesso

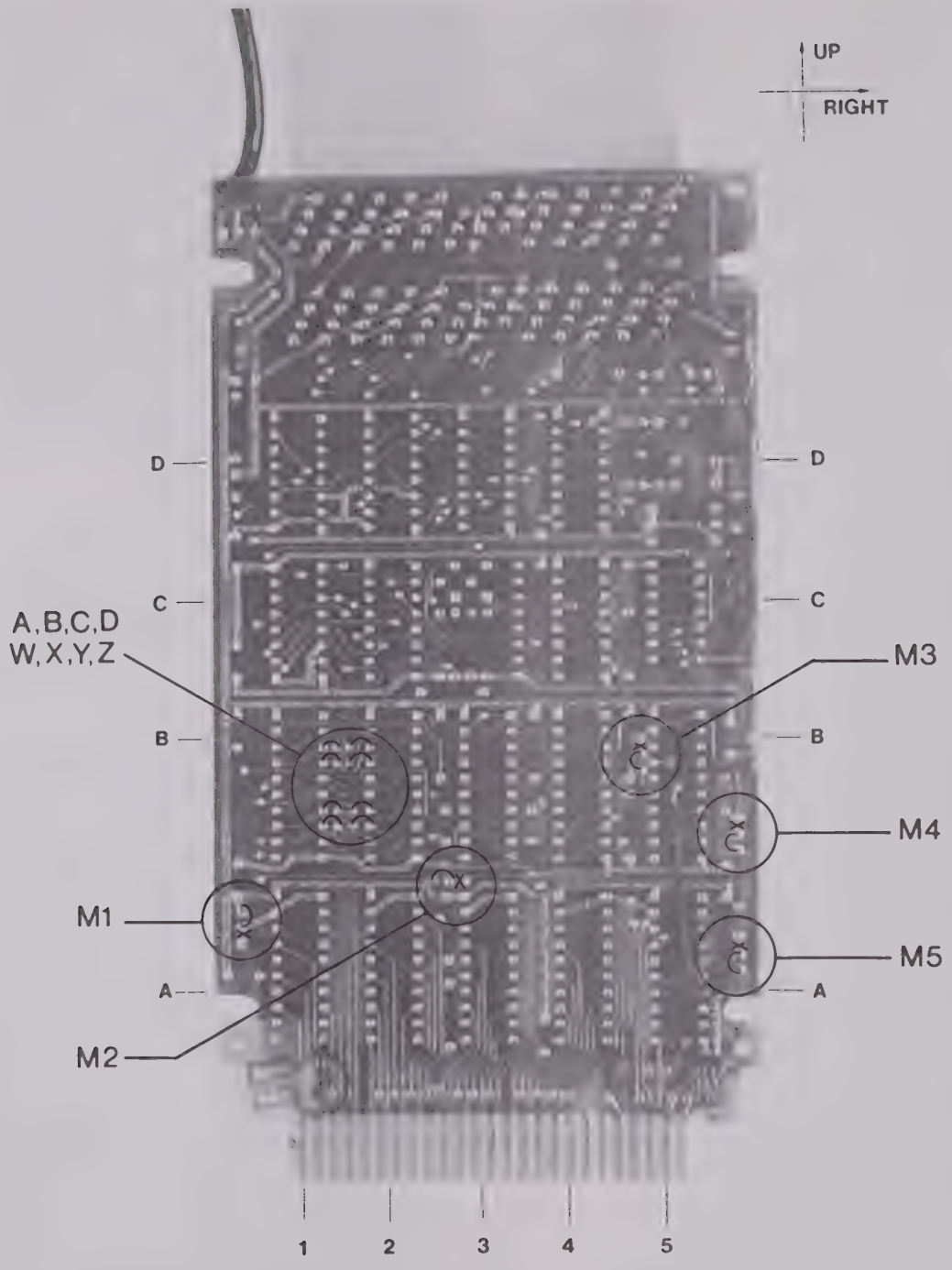


Figure 3.8 View of component side of K100-D/32 Input Adapter board. Jumper areas are etched on the board's surface.

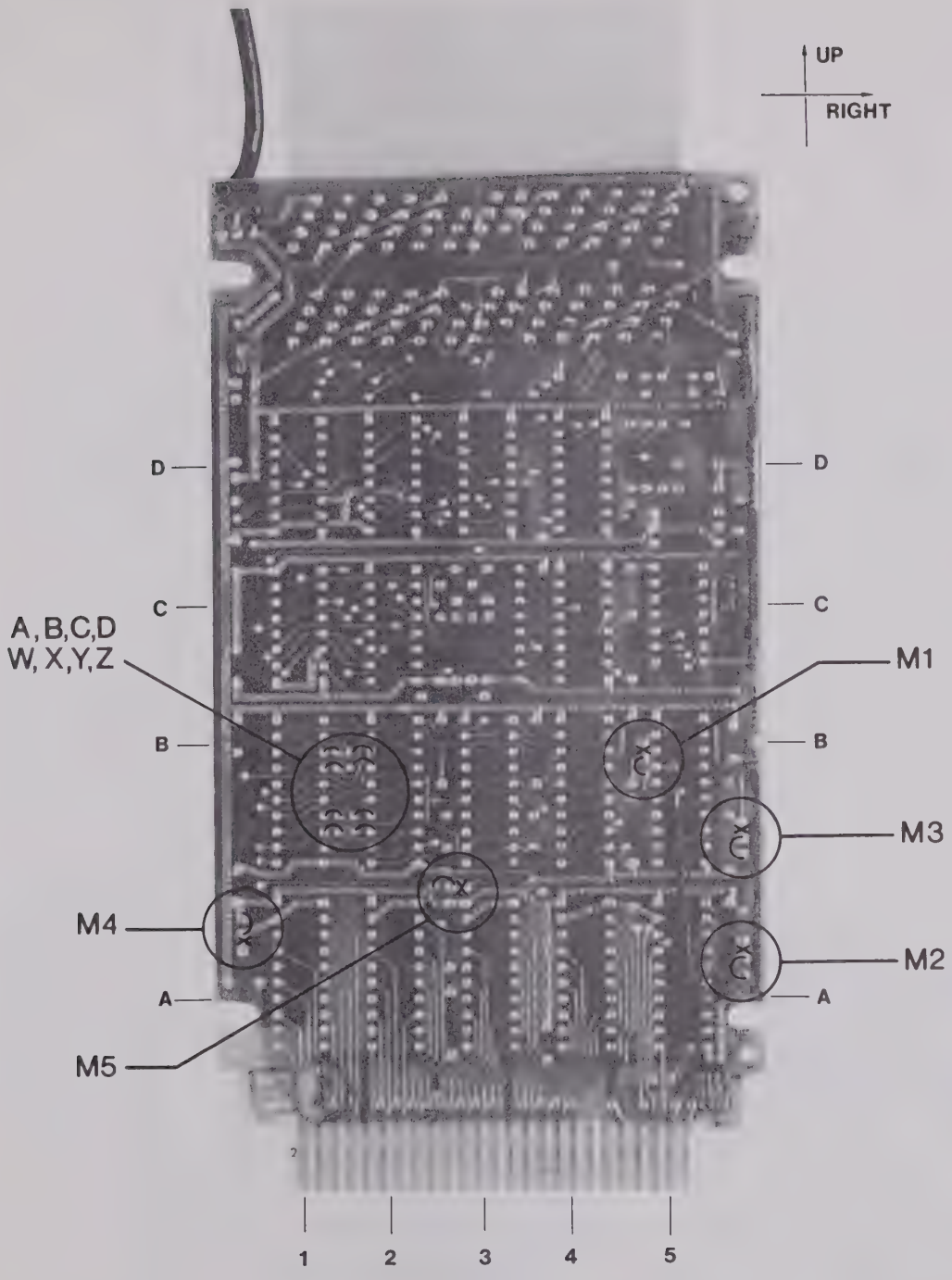


Figure 3.9 View of solder side of K100-D/32 Input Adapter board. This is the view referenced in Table 3.2.

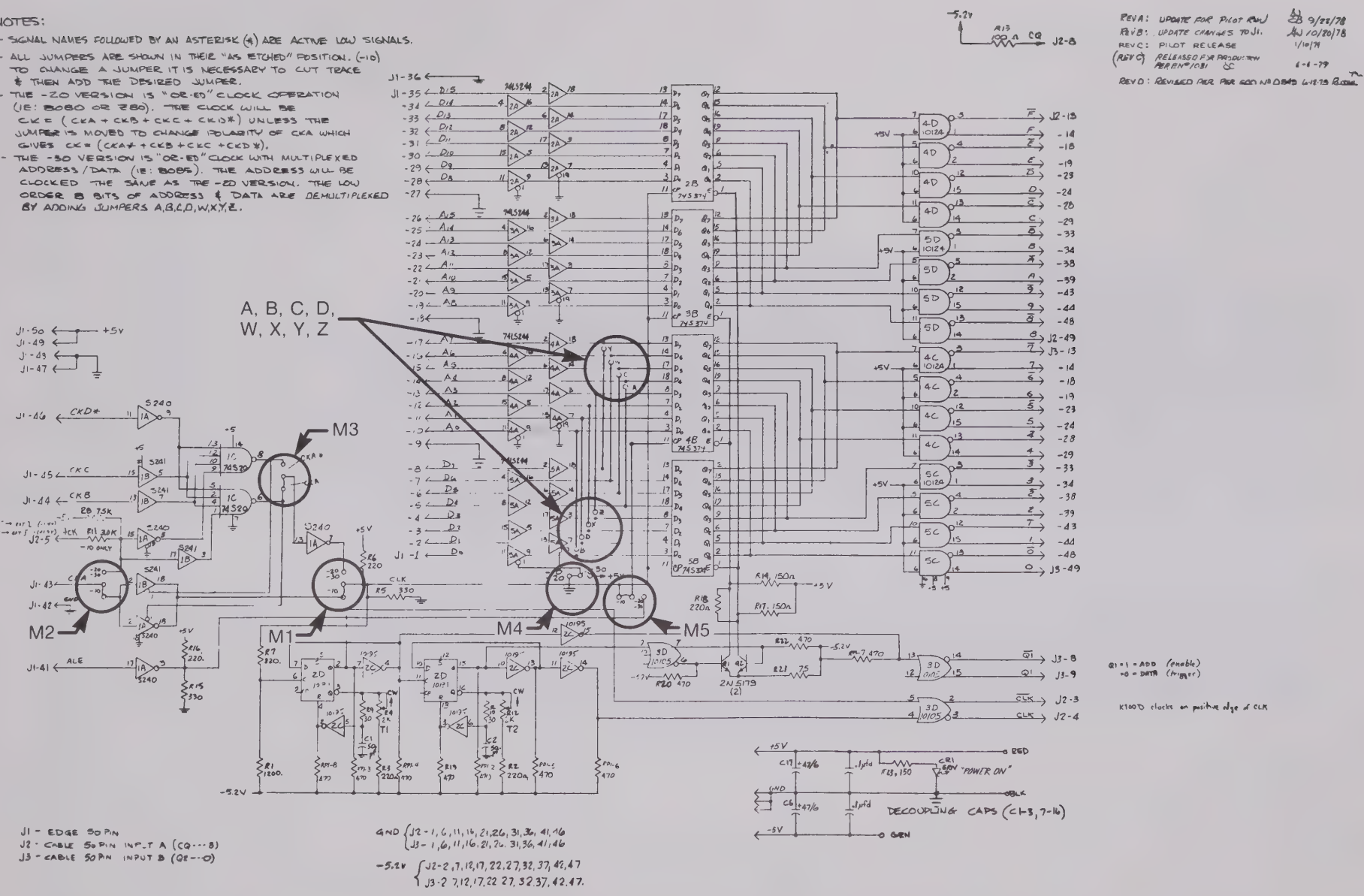

NOTES:
1- SIGNAL NAMES FOLLOWED BY AN ASTERISK (*) ARE ACTIVE LOW SIGNALS.
2- ALL JUMPERS ARE SHOWN IN THEIR "AS ETCHED" POSITION. (-10) TO CHANGE A JUMPER IT IS NECESSARY TO CUT TRACE & THEN ADD THE DESIRED JUMPER.
3- THE -2D VERSION IS "OR-ED" CLOCK OPERATION (IE: 8080 OR Z80). THE CLOCK WILL BE CLK = (CKA + CKB + CKC + CKD*) UNLESS THE JUMPER IS MOVED TO CHANGE POLARITY OF CKA WHICH GIVES CK = (CKA* + CKB + CKC + CKD*).
4- THE -3D VERSION IS "OR-ED" CLOCK WITH MULTIPLEXED ADDRESS/DATA (IE: 8085). THE ADDRESS WILL BE CLOCKED THE SAME AS THE -2D VERSION. THE LOW ORDER 8 BITS OF ADDRESS & DATA ARE DEMULTIPLEXED BY ADDING JUMPERS A,B,C,D,W,X,Y,Z.
REV A: UPDATE FOR PILOT RUN 9/28/78
REV B: UPDATE CHANGES TO J1. 10/20/78
REV C: PILOT RELEASE 1/10/79
(REV C) RELEASED FOR PRODUCTION PER ECN# 1081 SC 6-6-79
REV D: REVISED PER PER ECO NO 0845 6-18-79
A, B, C, D, W, X, Y, Z
M1
M2
M3
M4
M5
J1 - EDGE 50 PIN
J2 - CABLE 50 PIN INPUT A (CQ---8)
J3 - CABLE 50 PIN INPUT B (Q8---0)
GND {J2 - 1, 6, 11, 14, 21, 26, 31, 36, 41, 46
J3 - 1, 6, 11, 16, 21, 26, 31, 36, 41, 46
-5.2V {J2 - 2, 7, 12, 17, 22, 27, 32, 37, 42, 47
J3 - 2, 7, 12, 17, 22, 27, 32, 37, 42, 47
Q1 = 1 = ADD (enable)
=0 = DATA (inhibit)
K100-D clocks on positive edge of CLK
DECOUPLING CAPS (C1-3, 7-16)
"POWER ON"

Figure 3.10 K100-D/32 Input Adapter Schematic. Jumper areas for OR clocking and demultiplexing are circled and labeled as referenced in Table 3.2, Figure 3.8, and Figure 3.9.

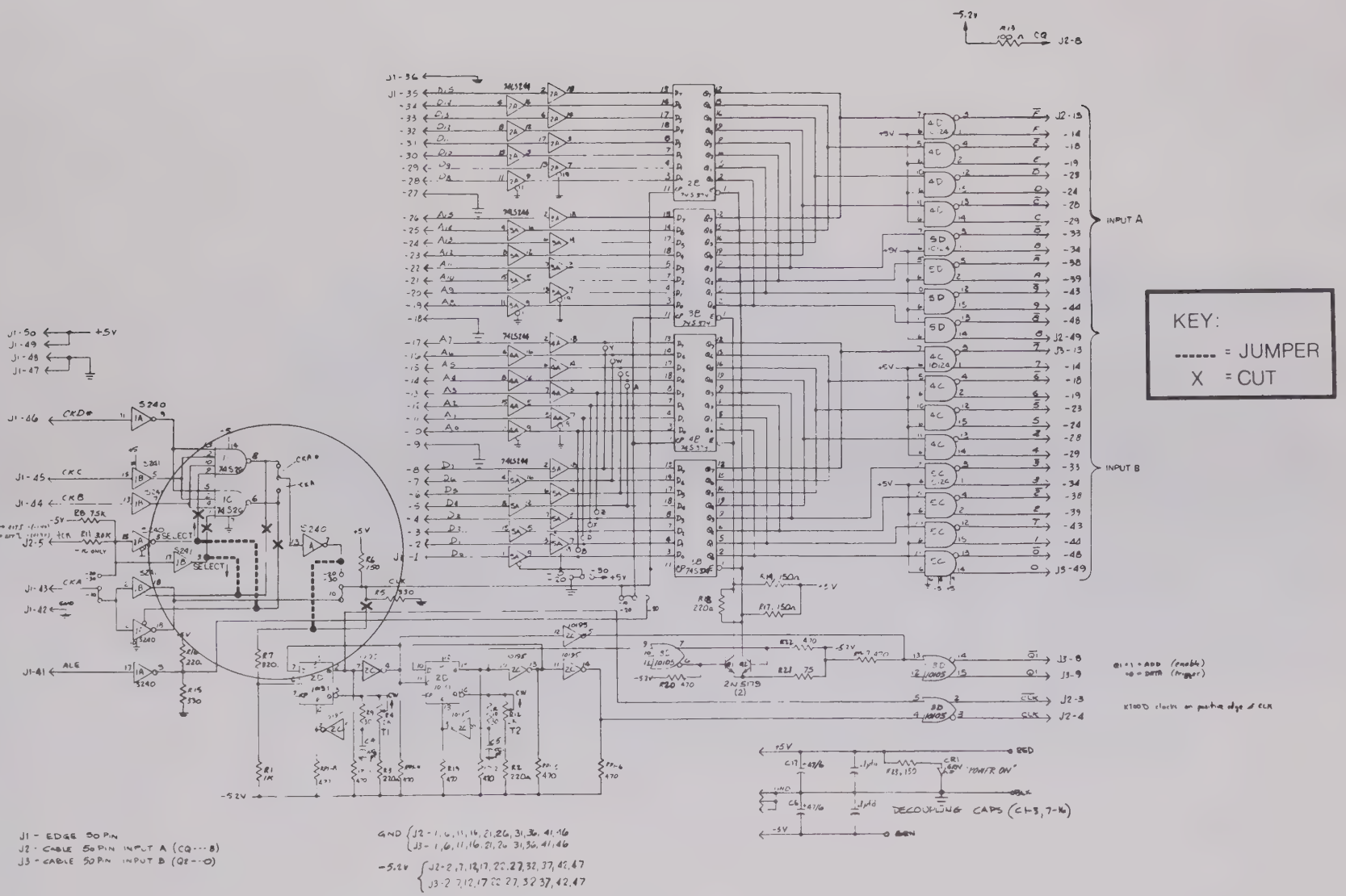


Figure 3.11. K100-D/32 Input Adapter Schematic. Modifications for Version 40 are contained within the circled area shown above.

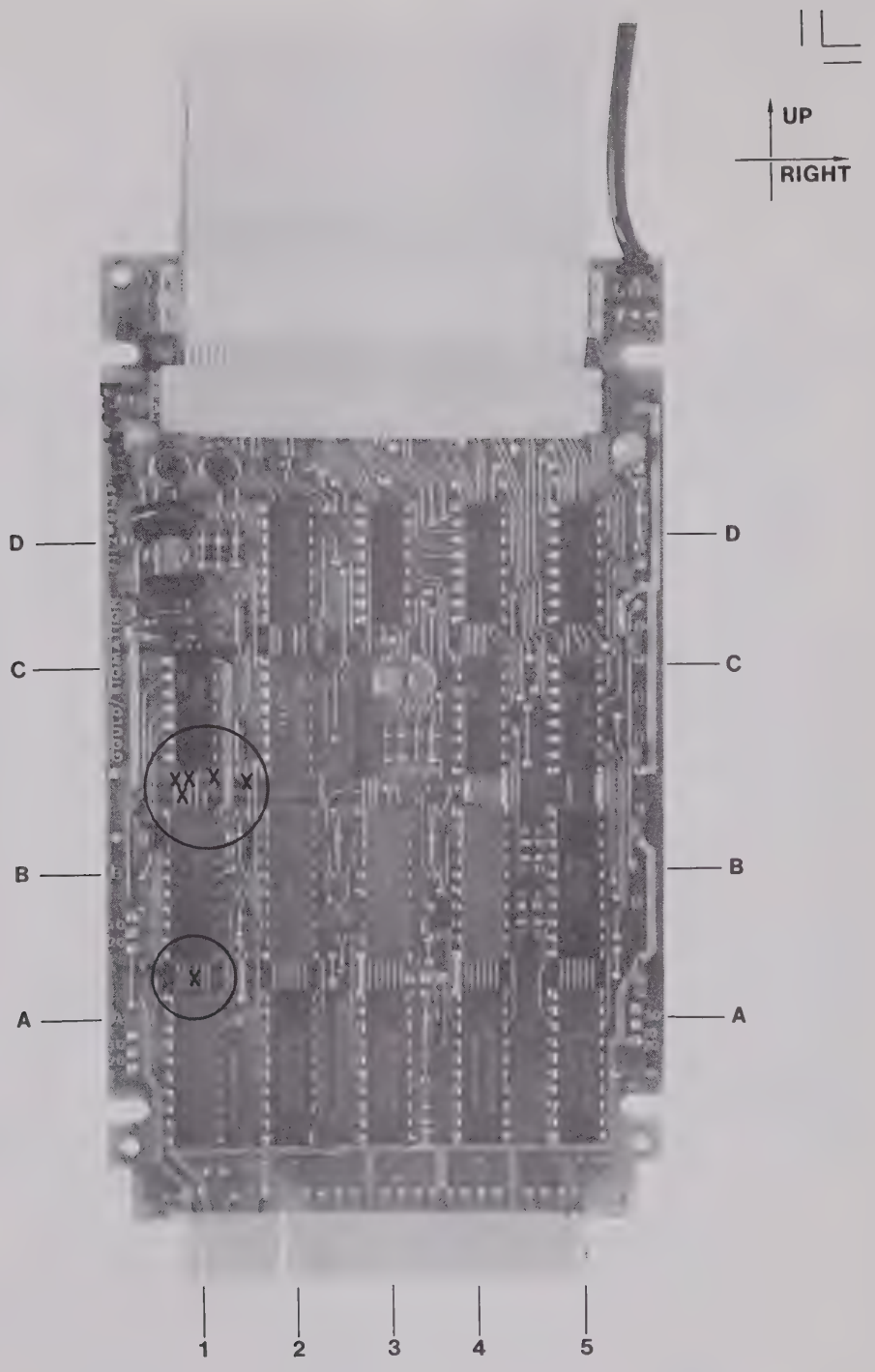


Figure 3.12 View of Component Side of K100-D/32 Channel Adapter Board Showing the Six Cuts Needed for Version 40 (Z-80) Operation

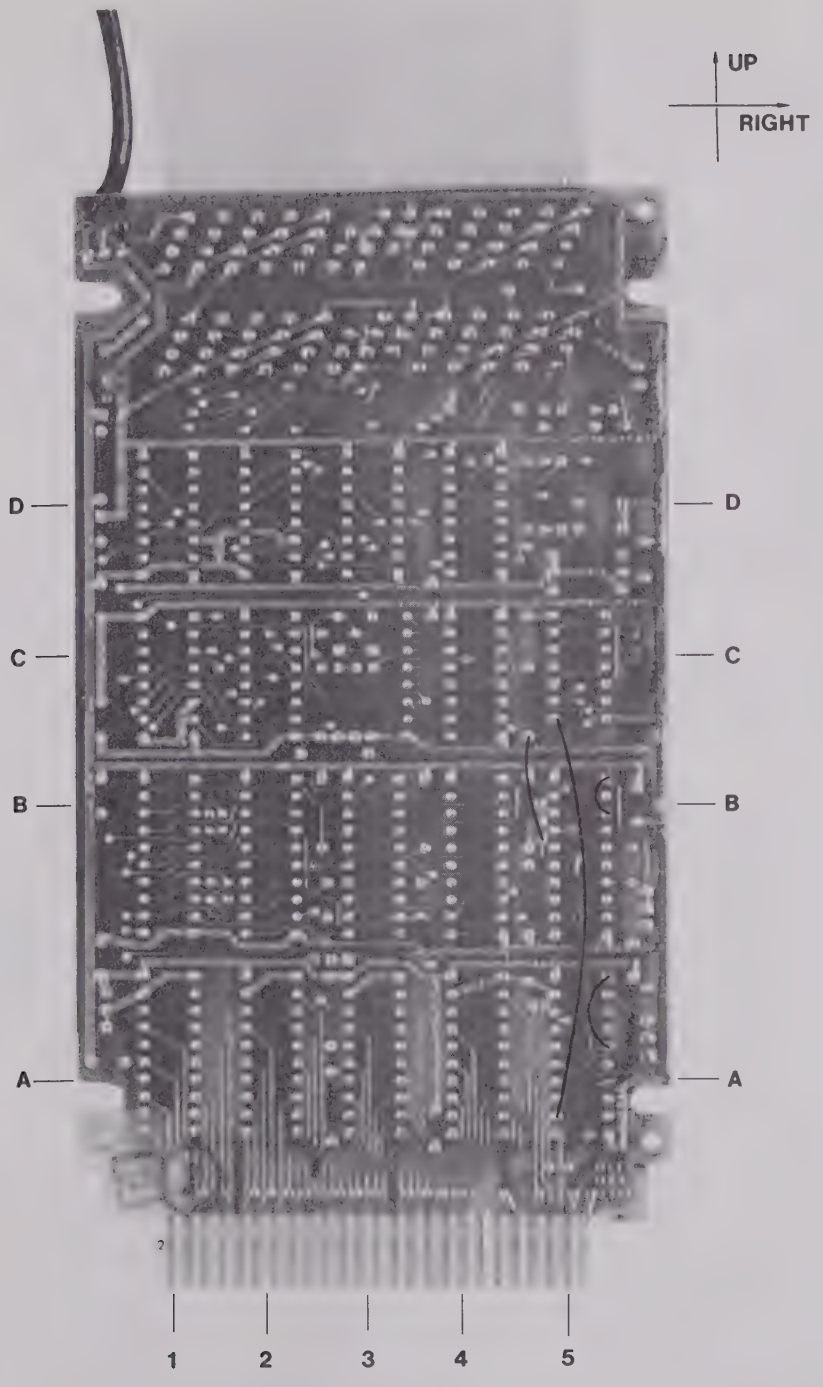
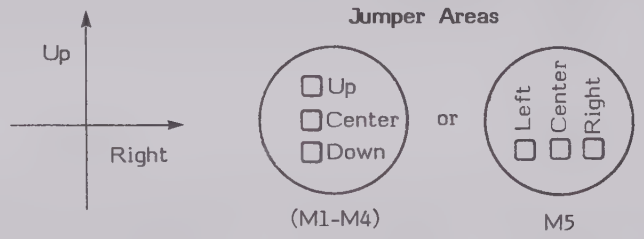


Figure 3.13 View of Solder Side of K100-D/32 Channel Input Adapter Board Showing the Four Jumpers Needed for Version 40 (Z-80) Operation

Table 3.2 K100-D/32 Input Adapter Modification Table

Version	Microprocessors	Comments	Primary Jumper Modifications[1] M1	M2	M3	M4	M5
10[2]	6800, 6802, 6809 2650.	Standard factory version. All clocks are ANDed. Edge of CKA is keyboard selectable.	Up	Up	Don't Care	Down	Right
20	8080, 8086, 8088	Clock signals are ORed. Edge of CKA is not keyboard selectable.	Down	Down	Up CKA[4] Down CKA*	Down	Right
30[3]	8085	OR clocking plus demultiplexing of lower address and data bytes.	Down	Down	Down	Up	Left
40	Z80, Z8002	Nonstandard jumpering. Refer to Section 3.4.3					

1. All jumper connections are referenced from the solder side of the adapter board with the cable connections at the top (Up) and the edge connector at the bottom (Down). The Primary Jumper connections should be made from the center point to the adjacent point indicated in the table (Up, Down, Right or Left). "Up," for example, means jumper Center to Up and cut Center to Down. This orientation is shown below and is duplicated in Figures 3.8 and 3.9.



2. No jumper modifications are necessary for Version 10. The jumper positions are shown for reference and to simplify remodification if desired.

3. The eight secondary jumper connections necessary to route the 8085 address and data bytes should be made to the nearest pin of the closest adjoining IC as illustrated:

Bottom View (Solder Side)

4. See Table 3.3

Table 3.3 Connection Guide Between Flying Leads of Adapter to Specific Microprocessors

Microprocessor			6800		6802		6809		6502		8080A		8088		8086		Z8002		8085		Z80	
K100-D/32 Input Adapter Version			10		10		10		10		20		20		20		20		30		40	
Flying Leads \ Clock Edge			⊄		⊄		⊄		⊄		X		X		X		X		X		X	
Pin #	Sleeve Marking	Sleeve Color	Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
1	D0	Yellow	33	D0	33	D0	31	D0	33	DB0	10	D0	26	SO($\overline{DEN}$)			21	STO			14	D0
2	D1	↑	32	D1	32	D1	30	D1	32	DB1	9	D1	27	S1(DT/$\overline{R}$)			20	ST1			15	D1
3	D2		31	D2	31	D2	29	D2	31	DB2	8	D2	28	S2(IO/$\overline{M}$)	17	NMI	19	ST2			12	D2
4	D3		30	D3	30	D3	28	D3	30	DB3	7	D3	38	A16/S3	18	INTR	18	ST3			8	D3
5	D4		29	D4	29	D4	27	D4	29	DB4	3	D4	37	A17/S4	21	RESET	25	R/$\overline{N}$			7	D4
6	D5		28	D5	28	D5	26	D5	28	DB5	4	D5	36	A18/S5	22	READY	26	N/$\overline{S}$			9	D5
7	D6	↓	27	D6	27	D6	25	D6	27	DB6	5	D6	35	A19/S6	23	TEST	27	B/$\overline{W}$			10	D6
8	D7	Yellow	26	D7	26	D7	24	D7	26	DB7	6	D7	34	$\overline{SS0}$	26	$\overline{SO}$ ($\overline{DEN}$)	17	DS			13	D7
9	None	Black																				
10	A0	White	9	A0	9	A0	8	A0	9	AB0	25	A0	16	AD0	16	AD0	40	AD0	12	AD0	30	A0
11	A1	↑	10	A1	10	A1	9	A1	10	AB1	26	A1	15	AD1	15	AD1	32	AD1	13	AD1	31	A1
12	A2		11	A2	11	A2	10	A2	11	AB2	27	A2	14	AD2	14	AD2	33	AD2	14	AD2	32	A2
13	A3		12	A3	12	A3	11	A3	12	AB3	29	A3	13	AD3	13	AD3	34	AD3	15	AD3	33	A3
14	A4		13	A4	13	A4	12	A4	13	AB4	30	A4	12	AD4	12	AD4	35	AD4	16	AD4	34	A4
15	A5		14	A5	14	A5	13	A5	14	AB5	31	A5	11	AD5	11	AD5	36	AD5	17	AD5	35	A5
16	A6	↓	15	A6	15	A6	14	A6	15	AB6	32	A6	10	AD6	10	AD6	37	AD6	18	AD6	36	A6
17	A7	White	16	A7	16	A7	15	A7	16	AB7	33	A7	9	AD7	9	AD7	38	AD7	19	AD7	37	A7
18	None	Black																				
19	A8	Yellow	17	A8	17	A8	16	A8	17	AB8	34	A8	8	A8	8	AD8	39	AD8	21	A8	38	A8
20	A9	↑	18	A9	18	A9	17	A9	18	AB9	35	A9	7	A9	7	AD9	1	AD9	22	A9	39	A9
21	A10		19	A10	19	A10	18	A10	19	AB10	1	A10	6	A10	6	AD10	2	AD10	23	A10	40	A10
22	A11		20	A11	20	A11	19	A11	20	AB11	40	A11	5	A11	5	AD11	3	AD11	24	A11	1	A11
23	A12		22	A12	22	A12	20	A12	22	AB12	37	A12	4	A12	4	AD12	4	AD12	25	A12	2	A12
24	A13		23	A13	23	A13	21	A13	23	AB13	38	A13	3	A13	3	AD13	5	AD13	26	A13	3	A13
25	A14	↓	24	A14	24	A14	22	A14	24	AB14	39	A14	2	A14	2	AD14	9	AD14	27	A14	4	A14
26	A15	Yellow	25	A15	25	A15	23	A15	25	AB15	36	A15	39	A15	39	AD15	8	AD15	28	A15	5	A15
27	None	Black																				
28	D8	Yellow	34	R/$\overline{W}$	34	R/$\overline{W}$	32	R/$\overline{W}$	34	R/$\overline{W}$	16	INTE	17	NMI	27	S1(DT/$\overline{R}$)	11	$\overline{VI}$	29	S0	27	M1
29	D9	↑	4	$\overline{IRQ}$	4	$\overline{IRQ}$	3	$\overline{IRQ}$	4	$\overline{IRQ}$	14	INT	18	INTR	28	S2(M/$\overline{IO}$)	12	$\overline{NVI}$	33	S1	20	$\overline{IORQ}$
30	D10		6	$\overline{NMI}$	6	$\overline{NMI}$	4	$\overline{FIRQ}$	6	$\overline{NMI}$	13	HOLD	31	HOLD	16	A0	13	$\overline{NMI}$	34	IO/$\overline{M}$	19	$\overline{MREQ}$
31	D11		2	$\overline{HALT}$	2	$\overline{HALT}$	2	NMI	2	RDY(IN)	21	HLDA	30	HLDA	34	BHE/S7	14	$\overline{RESE}$	10	INTR	21	$\overline{RD}$
32	D12		40	$\overline{RESET}$	40	$\overline{RESET}$	37	$\overline{RESET}$	40	$\overline{RESET}$	12	RESET	21	RESET	38	A16/S3	23	$\overline{WAIT}$	7	RST7.5	26	$\overline{RESET}$
33	D13		39	TSC	36	RE	6	BA	7	SYNC	23	READY	22	READ	37	A17/S4	6	$\overline{STOP}$	8	RST6.5	24	$\overline{WAIT}$
34	D14		7	BA	7	BA	5	BS	38	SO	24	WAIT	23	$\overline{TEST}$	36	A18/S5	22	$\overline{BURSQ}$	9	RST5.5	16	$\overline{INT}$
35	D15	Yellow	36	DBE	3	MR	33	DMA/$\overline{BREQ}$			17	DBIN	29	$\overline{WR}$(LOCK)	35	A19/S6	24	$\overline{BUSAK}$	6	TRAP	17	$\overline{NMI}$
36	None	Black																				
37																						
38																						
39																						
40																						
41	ALE	Blue																	30	ALE		
42	None	Black	1	Vss	1	Vss	1	Vss	1	Vss	2	Vss	20	GND	20	GND	31	GND	20	GND	29	GND
43	CKA	Red	37	Ø2	37	E	34	E	39	Ø2			24	$\overline{INTA}$	24	$\overline{INTA}$	29	$\overline{AS}$	11	$\overline{INTA}$	6	Ø
44	CKB	↑	5	VMA	5	VMA							32	$\overline{RD}$	32	$\overline{RD}$	17	$\overline{DS}$	32	$\overline{RD}$	21	$\overline{RD}$
45	CKC	↕									18	$\overline{WR}$	29	$\overline{WR}$	29	$\overline{WR}$			31	$\overline{WR}$	22	WR
46	CKD	Red	21	Vss	21	Vss	1	Vss	21	Vss	17	DBIN	25	ALE	25	ALE	31	GND	20	GND	29	GND
47	None	Black	21	Vss	21	Vss	1	Vss	21	Vss	2	Vss	20	GND	20	GND	31	GND	20	GND	29	GND
48	None	Black																				
49																						
50																						

SECTION IV

PRINCIPLES OF OPERATION

4.1 Basic General Description

Refer to Figure 4.1 (Block Diagram), Figure 4.2 (Timing Diagram) and Schematic 0112-0136. Assume that the clock is selected for positive edge. Each positive edge of the clock causes the K100-D/32 to store the 32 lines of input data in the registers (745374) and starts the pulse generation circuit. This circuit generates two pulses in sequence. The first pulse clocks the address (16 inputs) into the K100-D. The second pulse disables the address information (3B and 4B) and enables the data information (2B and 5B) and then clocks the data information into the K100-D. After the second pulse, the registers will be enabled for the address information in readiness for the next clock. Thus the address information (16 lines) and the data information (16 lines) are multiplexed together by utilizing the tri-state control lines of the registers (745374).

The Input Data is buffered by the 74LS244's (locations 2A, 3A, 4A, and 5A) in order to provide high input impedance and also to delay the inputs. This delay reduces the hold-time required at the inputs. The hold-time (at the inputs) is equal to the hold-time of the register (745374) plus the delay of the clock buffer/inverter (745240 or 745241) minus the delay of the data buffers (74LS244).

4.2 Clock Selection and Qualification

The clock circuit is configured to allow the minimum possible delay for the clock input. This is accomplished by "collectoring" an inverter (745240) and a non-inverter (745241) and using the tri-state control lines to select which is used. The tri-state control line also allows for qualification by CKB, CKC, and CKD (by I.C. 1C). Thus, the inverter (1A - 1B) will be enabled if the negative edge was selected and CKB is high and CKC is high and CKD is low; or, the non-inverter (1B - 1B), will be enabled if the positive edge is selected and CKB is high and CKC is high and CKD is low. If the qualifiers are not correct, neither will be enabled and the CLK line will be held at the high level by the resistors R5 and R6.

4.3 Pulse Generation

The pulse generation circuit consists of two "one-shots" and is implemented in the ECL in order to get the required timing. Each "one-shot" is formed by an edge triggered D-type flip-flop (10131), an R-C network, and an inverter. The sample clock (CLK), is translated from TTL to ECL by the resistors R7 and R1 and applied to the flip-flop (2D-6). This causes the output to be set true ("1" at 2D-2 and "0" at 2D-3) and the capacitor (C1) begins to discharge. When the capacitor gets to the threshold (-1.3 volts) of the inverter, then the inverter output goes high and resets the flip-flop (2D-2 goes low and 2D-3 goes high). The capacitor (C1) is recharged. The rate of discharge for C1 is determined by the sum of R9 (30 ohms), R3 (220 ohms) and R4 (0-2K pot) and the rate of charge is determined by R9 and the output impedance of 2D-3 (about 7 ohms).

When the flip-flop is reset, 2D-2 goes low and the inverter output (2C-4) goes high, which clocks the second flip-flop and starts the second one-shot. The capacitor C2 and the resistors R10, R2, and R12 determine the time of the second one-shot.

Figure 4.2 shows the typical operation of this circuit. This timing set-up guarantees at least 10 ns of set-up time for the data going into the K100-D.

The first one-shot (T1) provides delay for the initial acquisition of the data by the register (745374). The second one-shot (T2) causes the data to be switched on and delayed long enough for the registers to be switched. The address information is transferred to the K100-D at the end of T1 and the data information is transferred at the end of T2.

The signal T1 is delayed about 5 ns by two inverters and transferred to the Q1 input of the K100-D. This allows the K100-D to distinguish between address information (Q1=high) and data information (Q1=low). This operation is handled automatically by the software in the K100-D as follows: when the address trigger combination (TRIG ADRS) is transferred from software to hardware, the Q1 bit is set to "1" and when the data trigger combination (TRIG DATA) is transferred, the Q1 bit is set to "0".

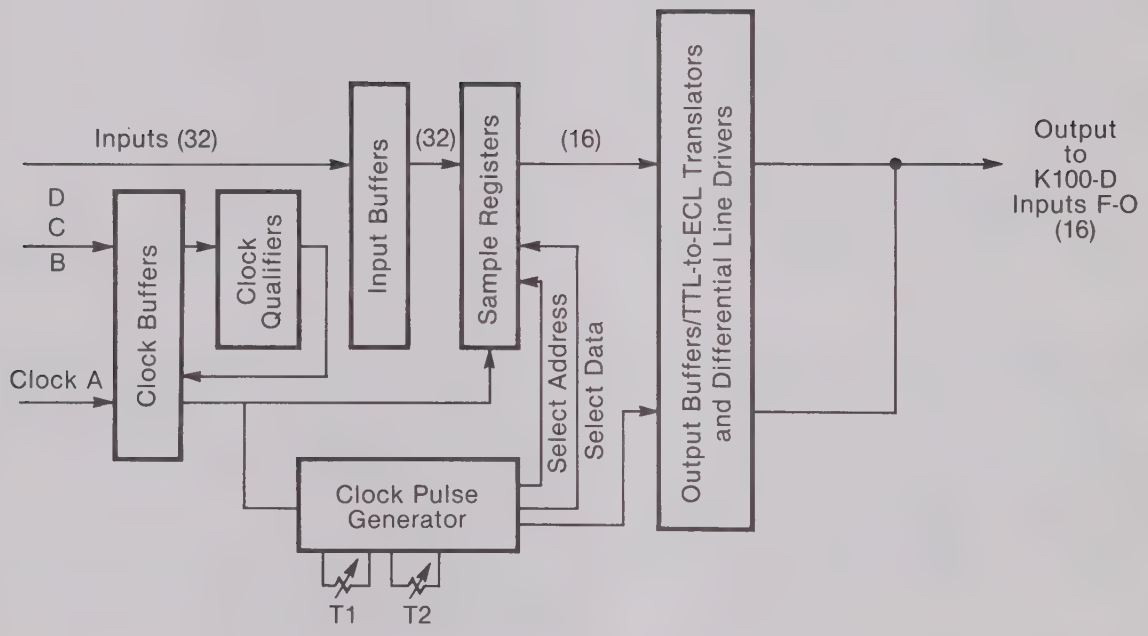


Figure 4.1 Block Diagram

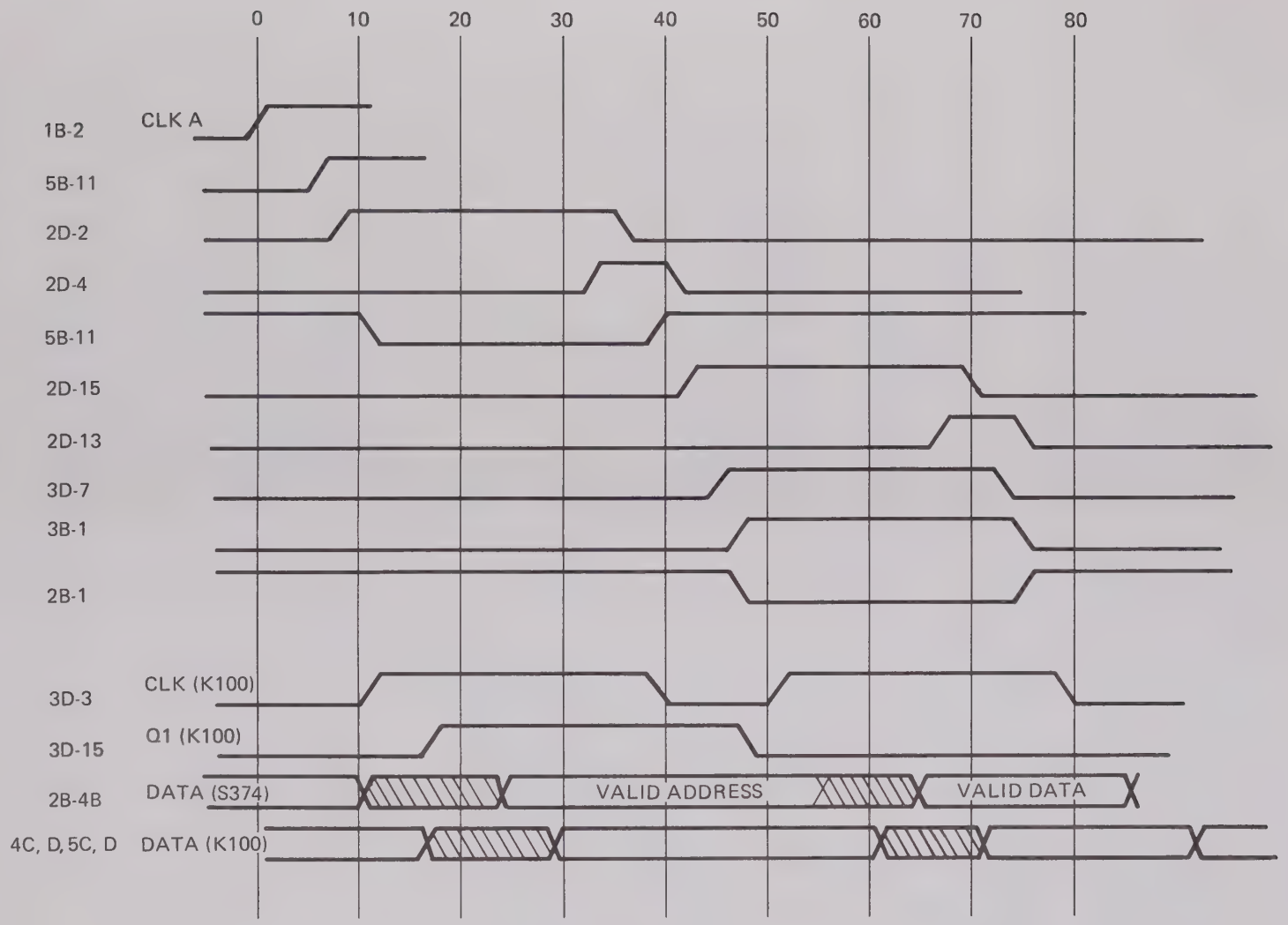


Figure 4.2 K100-D/32 Timing Diagram

4.4 Options

As noted on the schematic (0112-0136), provisions are made for two other options of clock operation which may be selected by modifying the PC board. Option 20 allows for "ORed CLOCK" operation (as needed for 8080 or Z80). Option 30 allows for demultiplexing the least significant eight bits of address and data (as needed for 8085 operation). These clock options cause more delay (about 5 ns) of the clock signal and thus increase the required hold-time of the data at the inputs and decrease the required set-up time. For a more detailed description, refer to Section 3.4.

SECTION V

CALIBRATION PROCEDURES

5.1 Recalibration of Internal Circuits

The following calibration procedure is to be used in recalibrating the internal circuits of the Model K100-D/32 Input Adapter. The unit was calibrated before shipment and should not require any re-calibration for at least six months or 1,000 hours of operation.

5.2 Required Test Equipment

The following test equipment is required to calibrate the Model K100-D/32 Input Adapter.

1. 250-MHz oscilloscope; two channels with horizontal resolution to 1 ns (Tektronix 475A).
2. Two pulse generators; square waves up to 20 MHz with less than a 5 ns rise time (Tektronix PG502).
3. Model K100-D Digital Logic Analyzer.

5.3 Power Supply Verification

Refer to Figure 5.1 while performing the following procedure.

Remove the top and bottom covers of the unit via four screws located on the bottom cover. Plug in the power cable connector into the rear of the Model K100-D Logic Analyzer and verify that +5 V and -5.2 V are present at the PCB. The red wire is +5 V, the black wire is ground, and the green wire is -5.2 V.

Voltage	Range
+5 VDC	±50 mV
-5.2 VDC	±50 mV

5.4 Adjustments

Unless otherwise specified, the following connections are to be maintained.

5.4.1 Connect a 12 MHz TTL clock to input ribbon cable pin J1-43 (CKA).

5.4.2 Plug in output ribbon cable connectors J2 and J3 into their respective places on the front panel of the Model K100-D Logic Analyzer. Plug in power cable into rear of K100-D.

5.4.3 Connect J1-46 (CKD*) to ground.

5.4.4 Leave J1-45 (CKC) and J1-44 (CKB) lines open so that they float to TTL logic high levels.

5.4.5 Monitor 2D-2 with channel 1 of oscilloscope (ECL level). Trigger off of channel 1. Adjust T1 for pulse width of 28-30 ns, measured at ECL threshold of -1.3 V.

5.4.6 Monitor 2D-15 with channel 1 of oscilloscope (ECL level). Adjust for pulse width of 28-30 ns, measured at ECL threshold of -1.3 V.

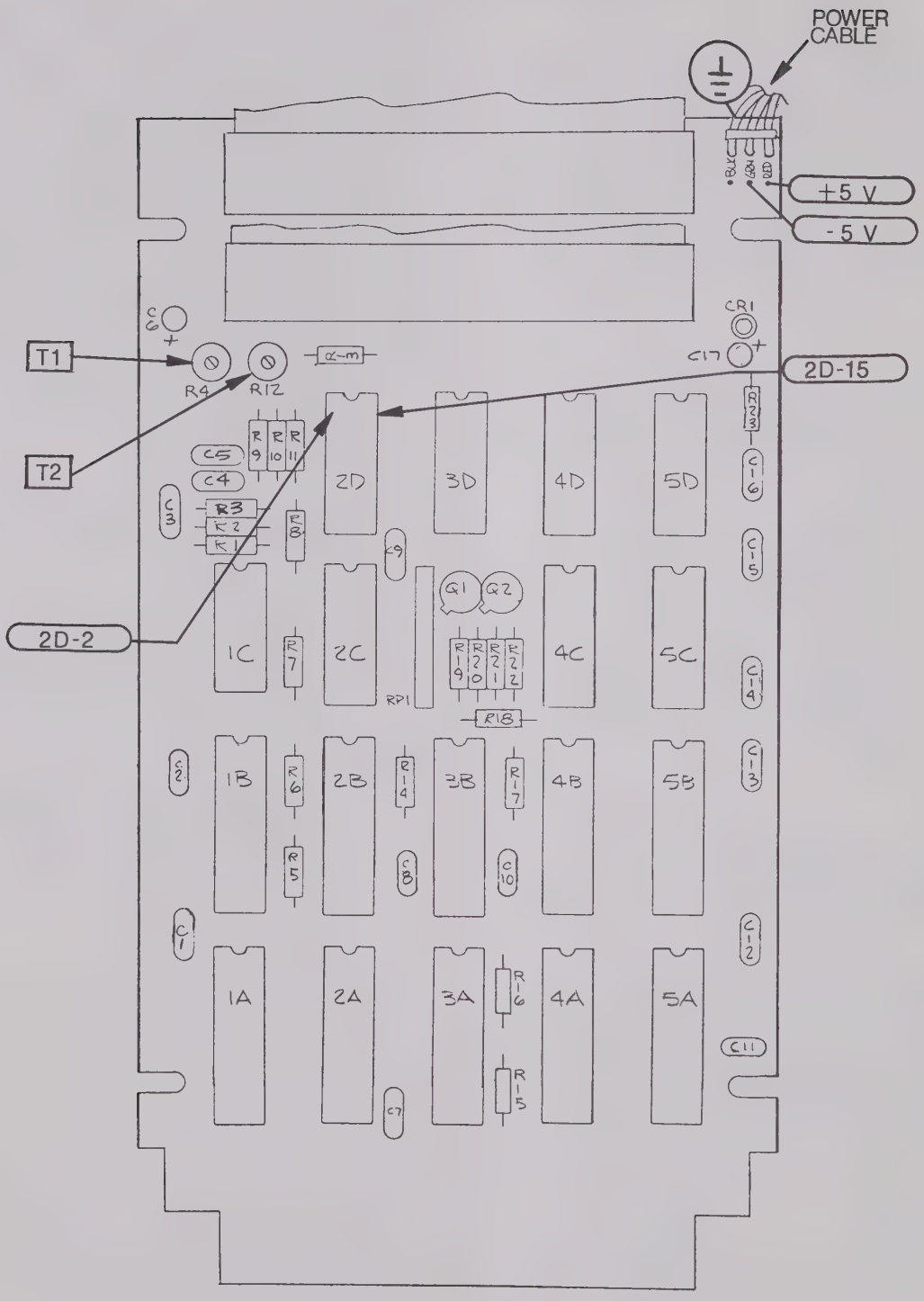


Figure 5.1 K100-D/32 Input Adapter Component Placement

SECTION VI

MAINTENANCE

6.1 Introduction

This section covers the Model K100-D/32 Input Adapter diagnostic routine. Repair of the board can be performed with the aid of the technical description in Section IV as well as the diagnostic routine in this section.

The drawings in Section VII have been included to aid service personnel who wish to troubleshoot to the component level. Additional assistance regarding a particular problem can be obtained by contacting the Customer Service Department at the factory: Phone (408) 988-6800, TWX 910-338-0509.

6.2 Functional Checkout Dash 10 Configuration

The following procedure checks all of the address and data input buffers, operation of the latches, and TTL-to-ECL translators. This procedure verifies the standard dash 10 configuration.

6.2.1 Connect the Model K100-D/32 Input Adapter input cable pin J1-43 (CKA) to a 5 MHz TTL clock source. CKA ground must be connected to TTL generator ground. Connect J1-46 (CKD*) to ground.

6.2.2 Leave all address and data lines open at input ribbon cable J1 so that they float to a TTL logic high level.

6.2.3 Set K100-D Address and Data Trigger words for all 1 s. Press [STATUS] [ENABLE] [F] (4 times) [TRIGGER] [F] (4 times) [ENTR.]

6.2.4 Press [AUTO ARM] switch, then [DATA.] Verify trigger condition is correct with all hexadecimal Fs in all locations and no data jitter.

6.2 Functional Checkout (Cont.)

6.2.5 Ground data line DØ. Set K100-D Trigger word to FFFE. Refer back to 6.2.3 for trigger entry method. Verify that the data displayed is FFFE, and that address displayed is still FFFF.

6.2.6 Remove DØ and ground D1. Verify that data is FFFD with Data Trigger word set to FFFD. Use same method of entering trigger words for address and data.

6.2.7 Remove D1 and ground D2. Verify FFFB with Data Trigger of FFFB.

6.2.8 Remove D2 and ground D3. Verify FFF7 with Data Trigger of FFF7.

6.2.9 Remove D3 and ground D4. Verify FFEF with Data Trigger of FFEF.

6.2.10 Remove D4 and ground D5. Verify FFDF with Data Trigger of FFDF.

6.2.11 Remove D5 and ground D6. Verify FFBF with Data Trigger of FFBF.

6.2.12 Remove D6 and ground D7. Verify FF7F with Data Trigger of FF7F.

6.2.13 Remove D7 and ground D8. Verify FEFF with Data Trigger of FEFF.

6.2.14 Remove D8 and ground D9. Verify FDFF with Data Trigger of FDFF.

6.2.15 Remove D9 and ground D10. Verify FBFF with Data Trigger of FBFF.

6.2.16 Remove D10 and ground D11. Verify F7FF with Data Trigger of F7FF.

6.2 Functional Checkout (Cont.)

6.2.17 Remove D11 and ground D12. Verify EFFF with Data Trigger of EFFF.

6.2.18 Remove D12 and ground D13. Verify DFFF with Data Trigger of DFFF.

6.2.19 Remove D13 and ground D14. Verify BFFF with Data Trigger of BFFF.

6.2.20 Remove D14 and ground D15. Verify 7FFF with Data Trigger of 7FFF.

6.2.21 Remove D15 and follow the same procedure outline above for all of the address lines. Set Address Trigger word on K100-D to same as outline above.

6.2.22 The following procedure checks the operation of the clock qualifiers CKB and CKC. Turn off K100-D. Input a 10 MHz TTL square wave into the 32-channel adapter input cable pin J1-43 (CKA). Synchronize the second pulse generator to the 10 MHz generator. Set the output rate to 5 MHz (TTL) level).

NOTE: The following circuity in Figure 6.1 accomplishes the same purpose as the second pulse generator.

6.2.23 With the 5 MHz signal's rising edge lining up with the 10 MHz clock's rising edge, input the 5 MHz signal to input connector pin J1-44 (CKB).

Set K100-D Address and Data Trigger words for all 1 s. Press CLOCK EXT ENTR AUTO ARM DATA. Verify that data displayed are all hexadecimal Fs.

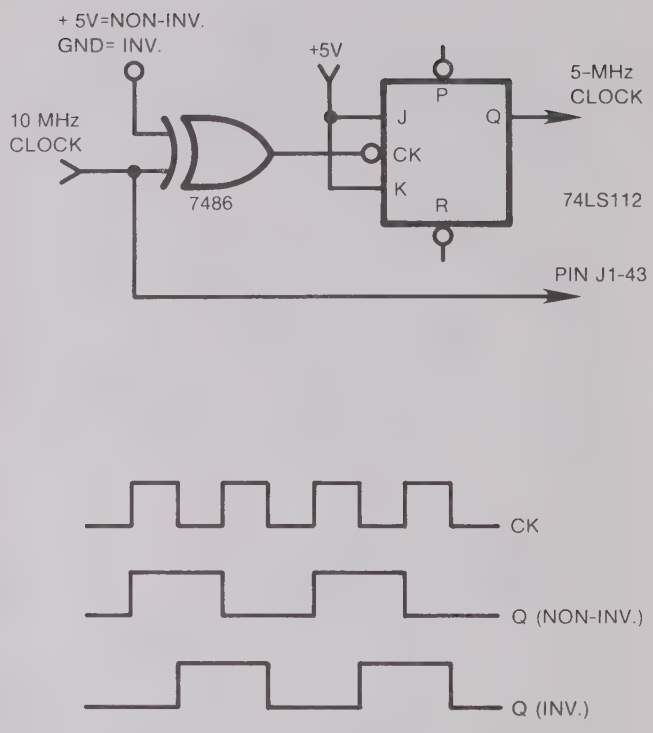


Figure 6.1 Alternate method of checking clock qualifier operation.

6.2.24 Convert the rising edge of the 5 MHz clock to correspond with the falling edge of the 10 MHz clock.

Press CLOCK EXT ENTR AUTO ARM DATA. Verify that all hexadecimal Fs are displayed.

6.2.25 Input the 5 MHz clock into input connector pin J1-45 (CKC). Repeat step 6.2.23 for pin J1-45 (CKC).

6.2.26 Repeat step 6.2.24 for pin J1-45 (CKC).

This completes the functional check of the Model K100-D/32 Input Adapter (Dash 10).

6.3 Functional Checkout
Dash 20 Configuration

The following procedure checks all address and data input buffers, operation of the latches, and TTL to ECL translators. This procedure verifies the optional (20) configuration. See schematic (Section VII) for jumper and cut lists.

6.3.1 Connect the K100-D/32 input cable pin J1-43 (CKA) to a 5MHz TTL clock source. J1-42 (Ground) must be attached to pulse generator ground. Connect J1-46 (CKD*) to ground.

6.3.2 Leave all address and data lines open at input ribbon cable J1 so that they float to a TTL logic high level.

6.3.3 Set K100-D Address and Data Trigger words for all 1 s. Press [STATUS] [ENABLE] [F] (4 times), [TRIGGER] [F] (4 times) [ENTR].

6.3.4 Press [AUTO ARM] switch, then DATA . Verify trigger condition is correct with all hexadecimal Fs in all locations and no data jitter.

6.3.5 Place J1-46 (CKD*) in non-connected position (open). Press [AUTO ARM] switch. Verify CK? on K100-D (lower left of screen). Return to ground.

6.3.6 Place J1-45 (CKC) to ground. Verify CK? Remove ground.

6.3.7 Place J1-44 (CKB) to ground. Verify CK? Remove ground.

6.3.8 Ground data line DØ. Set K100D Trigger word to FFFE. Refer back to 6.2.3 for trigger entry method. Verify that the data displayed is FFFE, and that address displayed is still FFFF.

6.3.9 Remove DØ and ground D1. Verify that data is FFFD with Data Trigger word set to FFFD. Use same method of entering trigger words for address and data.

6.3.10 Remove D1 and ground D2. Verify FFFB with Data Trigger of FFFB.

6.3.11 Remove D2 and ground D3. Verify FFF7 with Data Trigger of FFF7.

6.3.12 Remove D3 and ground D4. Verify FFEF with Data Trigger of FFEF.

6.3.13 Remove D4 and ground D5. Verify FFEF with Data Trigger of FFEF.

6.3.14 Remove D5 and ground D6. Verify FFBF with Data Trigger of FFBF.

6.3.15 Remove D6 and ground D7. Verify FF7F with Data Trigger of FF7F.

6.3.16 Remove D7 and ground D8. Verify FEFF with Data Trigger of FEFF.

6.3.17 Remove D8 and ground D9. Verify FDFF with Data Trigger of FDFF.

6.3.18 Remove D9 and ground D10. Verify FBFF with Data Trigger of FBFF.

6.3.19 Remove D10 and ground D11. Verify F7FF with Data Trigger of F7FF.

6.3.20 Remove D11 and ground D12. Verify EFFF with Data Trigger of EFFF.

6.3.21 Remove D12 and ground D13. Verify DFFF with Data Trigger of DFFF.

6.3.22 Remove D13 and ground D14. Verify DFFF with Data Trigger of DFFF.

6.3.23 Remove D14 and ground D15. Verify 7FFF with Data Trigger of 7FFF.

6.3.24 Remove D15 and follow the same procedure outline above for all of the address lines. Set Address Trigger word on K100-D to same as outline above.

This completes the functional checkout of the Model K100-D/32 Input Adapter (Dash 20).

6.4 Functional Checkout Dash 30 Configuration

The following procedure checks all address and data input buffers, operation of the latches, and TTL to ECL translators. This procedure verifies the optional (-30) configuration. See schematic (Section VII) for jumper and cut lists.

6.4.1 Connect the K100-D/32 input cable pins J1-43 (CKA) to a 5 MHz TTL clock source. J1-42 (Ground) must be attached to pulse generator ground. Connect J1-46 (CKD*) to ground.

6.4.2 Leave all address and data lines open at input ribbon cable J1 so that they float to a TTL logic high level.

6.4.3 Set K100-D Address and Data Trigger words for all 1 s. Press [STATUS] [ENABLE] [F] (4 times), [TRIGGER] [F] (4 times) - [ENTR .]

6.4.4 Press [AUTO ARM] switch, then [DATA .] Verify trigger condition is correct with all hexadecimal Fs in all locations and no data jitter.

6.4.5 Place J1-46 (CKD*) in non-connected position (open). Press [AUTO ARM] switch. Verify CK? on K100-D (lower left of screen). Return to ground.

6.5.6 Place J1-45 (CKC) to ground. Verify CK? Remove ground.

6.4.7 Place J1-44 (CKB) to ground. Verify CK?. Remove ground.

6.4.8 Ground data line DØ. Set K100-D Trigger word to FFFF. Refer back to 6.2.3 for trigger entry method. Verify that the data displayed is FFFF and that address displayed is still FFFF.

6.4.9 Remove DØ and ground D1. Verify that data is FFFF with Data Trigger word set to FFFF. Use same method of entering trigger words for address and data.

6.4.10 Remove D1 and ground D2. Verify FFFF with Data Trigger of FFFF.

6.4.11 Remove D2 and ground D3. Verify FFFF with Data Trigger of FFFF.

6.4.12 Remove D3 and ground D4. Verify FFFF with Data Trigger of FFFF.

6.4.13 Remove D4 and ground D5. Verify FFFF with Data Trigger of FFFF.

6.4.14 Remove D5 and ground D6. Verify FFFF with Data Trigger of FFFF.

6.4.15 Remove D6 and ground D7. Verify FFFF with Data Trigger of FFFF.

6.4.16 Remove D7 and ground D8. Verify FFFF with Data Trigger of FFFF.

6.4.17 Remove D8 and ground D9. Verify FDFF with Data Trigger of FDFF.

6.4.18 Remove D9 and ground D9. Verify FDFF with Data Trigger of FDFF.

6.4.19 Remove D10 and ground D11. Verify F7FF with Data Trigger of F7FF.

6.4.20 Remove D11 and ground D12. Verify EFFF with Data Trigger of EFFF.

6.4.21 Remove D12 and ground D13. Verify DFFF with Data Trigger of DFFF.

6.4.22 Remove D13 and ground D14. Verify BFFF with Data Trigger of BFFF.

6.4.23 Remove D14 and ground D15. Verify 7FFF with Data Trigger of 7FFF.

6.4.24 Remove D15 and follow the same procedure outline above for all of the address lines. Set Address Trigger word on K100-D to same as above, but notice values will be as in Table 6.1.

Table 6.1 Verification of Address Lines

	ADDR	DATA
A_0 Ground (only)	FFFE	FFFE
A_1 Ground (only)	FFFD	FFFD
A_2 Ground (only)	FFFB	FFFB
A_3 Ground (only)	FFF7	FFF7
A_4 Ground (only)	FFEF	FFEF
A_5 Ground (only)	FFDF	FFDF
A_6 Ground (only)	FFBF	FFBF
A_7 Ground (only)	FF7F	FF7F
A_8 Ground (only)	FEFF	FEFF
A9 Ground (only)	FDFF	FDFF
A_{10} Ground (only)	FBFF	FBFF
A_{11} Ground (only)	F7FF	F7FF
A_{12} Ground (only)	EFFF	EFFF
A_{13} Ground (only)	DFFF	DFFF
A_{14} Ground (only)	BFFF	BFFF
A_{15} Ground (only)	7FFF	7FFF

This completes the functional check of the Model K100-D/32 Input Adapter (Dash 30).

SECTION VII

SCHEMATICS AND ASSEMBLY DRAWINGS

7.1 Introduction

This section contains the schematics and assembly drawings for the Model K100-D/32 Input Adapter. Parts lists are also included for convenience.

7.2 List of Drawings

Figure		Page
7.1	K100-D/32 Input Adapter Assembly 0112-0130	35
7.2	K100-D/32 Input Adapter 0112-0136	36
7.3	K100-D/32 Input Adapter PWB Assembly 0112-0135	37

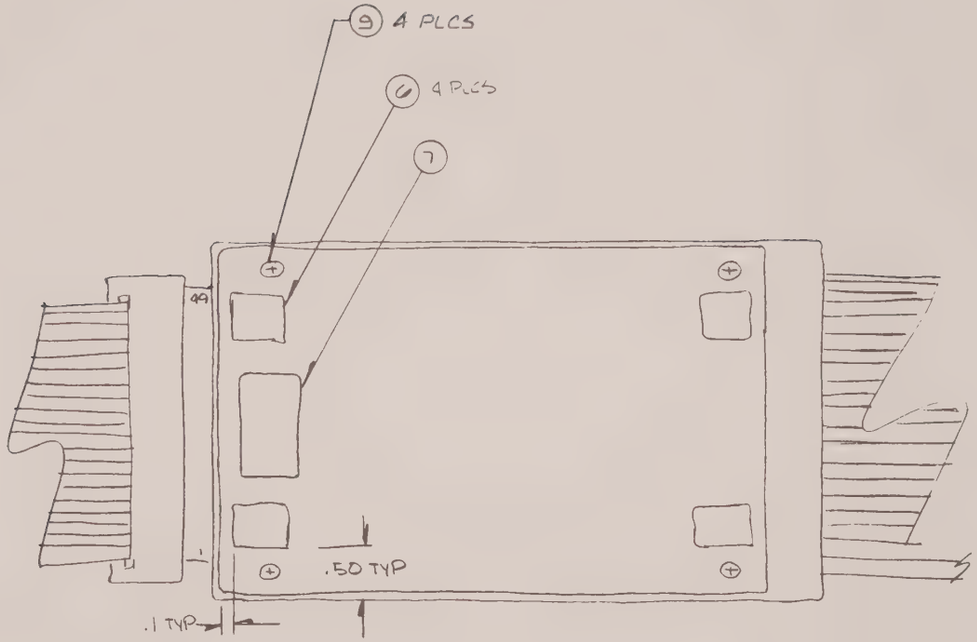
7.3 Parts Lists

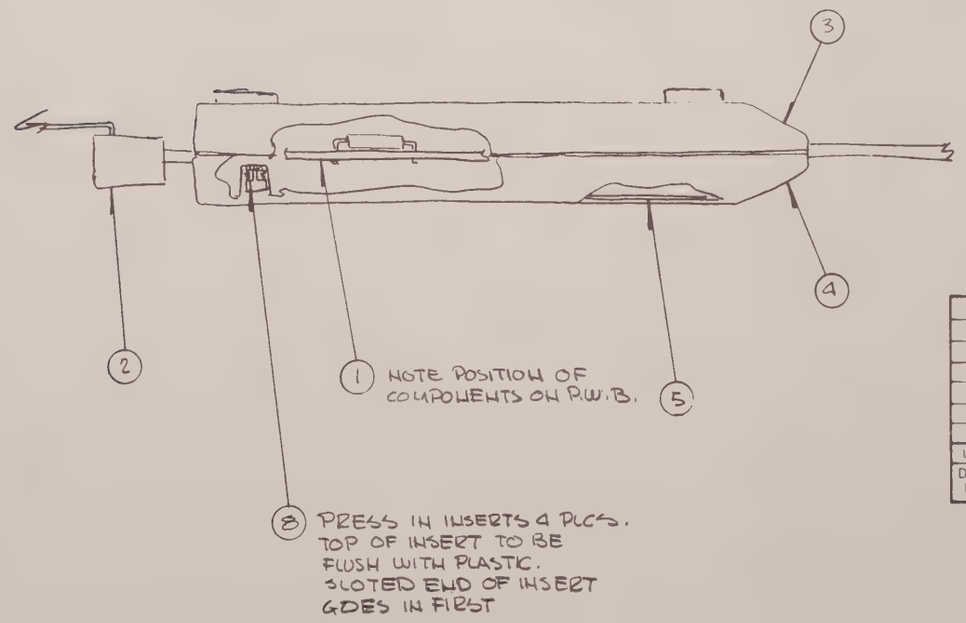
The materials in the following lists are subject to change without Gould Inc.'s prior notification. For list verification, contact the Customer Service Department at the factory: Phone (408) 988-6800, TWX 910-338-0509.

7.3.1 List of Parts Lists

Figure		Page
7.4	K100-D/32 Input Adapter Assembly 0112-0130	38
7.5	K100-D/32 Input Adapter PWB AssemblyAssembly 0112-0135	39

REV B: ADDED ITEM 9 PER ECO*159, 5-8-79, RDW
(REV B) RELEASED FOR PRODUCTION EN* 1081
6-6-79 - SLD




3
4
2
1 NOTE POSITION OF COMPONENTS ON P.W.B.
5
8 PRESS IN INSERTS 4 PLCS. TOP OF INSERT TO BE FLUSH WITH PLASTIC. SLOTED END OF INSERT GOES IN FIRST

																	3
																	2
																	1
						50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION SPECIFICATION				ITEM
						DO NOT SCALE DRAWING REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS ✓					DRAWN Buerkett	DATE 12-7-78	GOULD biomation				
						TOLERANCE DIMENSIONAL X ± .1 ANGLES XX ± .020 ° ' XXX .010 HOLE SIZE 0 599 ± .003 600 999 .004 1.000 ± 1.499 .005					CHECKED T McCann	1-8-78	TITLE 32 INPUT ADAPTER ASSY - K100				
											ENGINEER Curt Blandin	1-10-79					
						BEND RADIUS					MANUFACTURING Bucci	1/10/79	SCALE —	SIZE C	PART NUMBER 0112-0130		REV B
10	0112-0139	1				FINISH					QUALITY ASSUR	1/10/79	CODE		SHEET 1 OF 1		
DASH NO	NUMBER	QTY															
	NEXT ASSEMBLY																

Figure 7.1 K100-D/32 Input Adapter Assembly 0112-0130

NOTES:

1- SIGNAL NAMES FOLLOWED BY AN ASTERISK (*) ARE ACTIVE LOW SIGNALS.

2- ALL JUMPERS ARE SHOWN IN THEIR "AS ETCHED" POSITION. (-10) TO CHANGE A JUMPER IT IS NECESSARY TO CUT TRACE & THEN ADD THE DESIRED JUMPER.

3- THE -20 VERSION IS "OR-ED" CLOCK OPERATION (IE: 8080 OR Z80). THE CLOCK WILL BE CK = (CKA + CKB + CKC + CKD*) UNLESS THE JUMPER IS MOVED TO CHANGE POLARITY OF CKA WHICH GIVES CK = (CKA* + CKB + CKC + CKD*).

4- THE -30 VERSION IS "OR-ED" CLOCK WITH MULTIPLEXED ADDRESS/DATA (IE: 8085). THE ADDRESS WILL BE CLOCKED THE SAME AS THE -20 VERSION. THE LOW ORDER 8 BITS OF ADDRESS & DATA ARE DEMULTIPLEXED BY ADDING JUMPERS A,B,C,D,W,X,Y,Z.

REV A:	UPDATE FOR PILOT RUN	AB 9/22/78
REV B:	UPDATE CHANGES TO J1.	AW 10/20/78
REV C:	PILOT RELEASE	1/10/79
(REV C)	RELEASED FOR PRODUCTION PER ECN #1081	6-6-79
REV D:	REVISED PER ECO #0843	6-12-79 R.ODELL
REV E:	REVISED PER ECO #0944	10-12-79 J.CARROLL
REV F:	REVISED PER ECO #0010	10-2-79 J.CARROLL
REV G:	REVISED PER ECO #0	2-5-80 J.CARROLL
REV H:	REVISED PER ECO 1392	11-10-80 R.DEAN

J1 - EDGE 50 PIN
J2 - CABLE 50 PIN INPUT A (CQ---8)
J3 - CABLE 50 PIN INPUT B (Q2---0)

GND { J2 - 1,6,11,16,21,26,31,36,41,46
J3 - 1,6,11,16,21,26,31,36,41,46

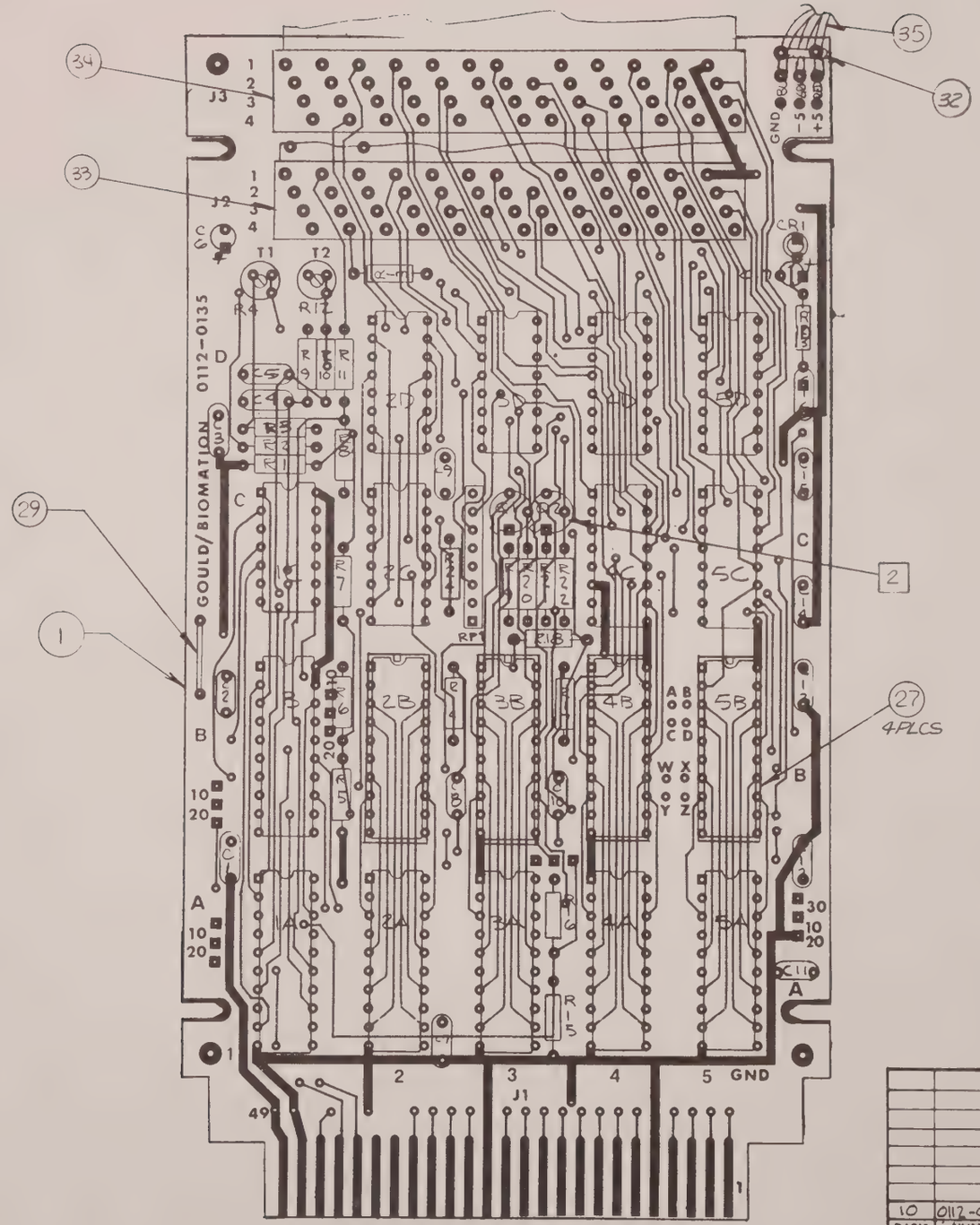
-5.2V { J2 - 2,7,12,17,22,27,32,37,42,47.
J3 - 2,7,12,17,22,27,32,37,42,47.

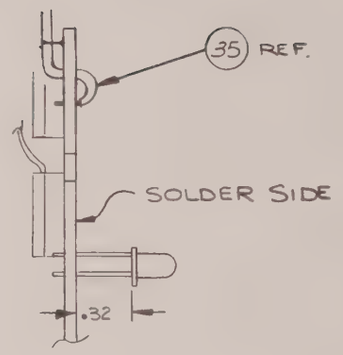
Q1 = 1 = ADD (enable)
=0 = DATA (trigger)

K100D clocks on positive edge of CLK

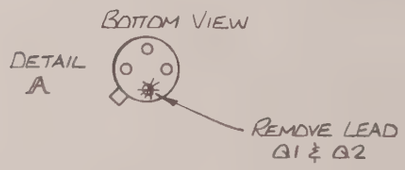
DRAWN C.Eberling	DATE 8-20-79	biomation	
CHECKED	10-29	TITLE SCHEMATIC - K100D/32 32 CHANNEL ADAPTOR	
ENGINEER C.Bloomfield	11-10-79		
MANUFACTURING	11/20/79	SCALE —	SIZE D
QUALITY ASSUR		PART NUMBER 0112-0136	REV H
		CODE	SHEET 1 OF 1

Figure 7.2 K100-D/32 Input Adapter 0112-0136





RED WIRE TO +5V
BLACK WIRE TO GND
GREEN WIRE TO -5.2V



REV B UPDATE CHANGES TO J1.
REV C PILOT RELEASE
(REV C) RELEASED FOR PRODUCTION PER EN# 1031 6-6-77 - SJC TM
REV D: REVISED PER ECO #849 6-14-78 S. RUDDELL
REV E: REVISED PER ECO No. 0856 7-16-79 CARROLL TM
REV F: REVISED PER ECO 0880 7-16-79 CARROLL TM
REV G: REVISED PER E.C.O# 0929 9-21-79 CARROLL TM
REV H: REVISED PER ECO N°0944 10-12-79 CARROLL TM
REV J: REVISED PER ECO No. 0970 10-15-79 CARROLL TM
REV K: PER E.C.O. 977 10-23-79 CARROLL TM
REV L: PER ECO 1392 2-23-81 BROWN

NOTES;
1) MAXIMUM COMPONENT HEIGHT ABOVE BOARD IS .32.
[2] REMOVE CASE GND LEAD FROM Q1 & Q2. (SEE DETAIL A)

									3
									2
									1
		50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

DO NOT SCALE DRAWING	DRAWN NANCY GAINES	DATE 6-14-78
REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS √	CHECKED T.W. Carroll	1-10-79
TOLERANCE: DIMENSIONAL X ± 1 ANGLES; XX ± 030 ±1°; XXX ± 010; HOLE SIZE 0 599 + 003, 600 999 + 004, 1 000 1 499 + 005	ENGINEER Curt Blanding	1-10-79
BEND RADIUS	MANUFACTURING Lucas	1/10/79
FINISH	QUALITY ASSUR Shannon D.	1/10/79

biomation

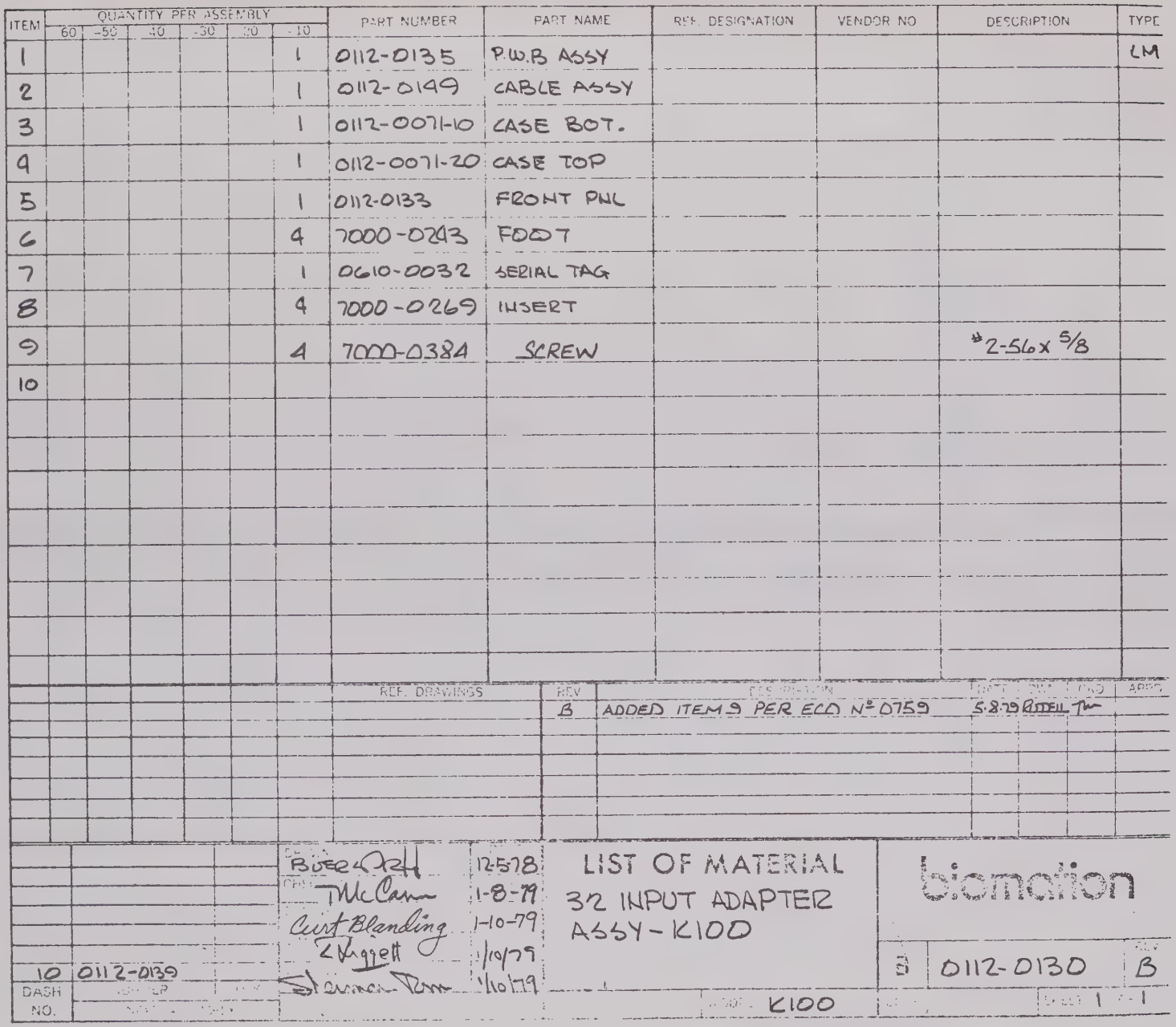
TITLE P.W.B. ASSEMBLY 32 CHANNEL ADAPT

SCALE	SIZE	PART NUMBER	REV
2/1	C	0112-0135	L

CODE | SHEET 1

DASH NO.	NUMBER	QTY
10	0112-0130	1
	NEXT ASSEMBLY	

Figure 7.3 K100-D/32 Input Adapter PWB Assembly 0112-0135



ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1						1	0112-0135	P.W.B ASSY				LM
2						1	0112-0149	CABLE ASSY				
3						1	0112-0071-10	CASE BOT.				
4						1	0112-0071-20	CASE TOP				
5						1	0112-0133	FRONT PNL				
6						4	7000-0243	FOOT				
7						1	0610-0032	SERIAL TAG				
8						4	7000-0269	INSERT				
9						4	7000-0384	SCREW			#2-56 x 5/8	
10												

REF. DRAWINGS	REV	DESCRIPTION	DRFT	CHK	ENG	APPD
	B	ADDED ITEM 9 PER ECO N° 0759	5-8-79 RUDELL			

DRFT	Bueerath	12-5-78	LIST OF MATERIAL 32 INPUT ADAPTER ASSY-K100
CHK	TMcCann	1-8-79	
ENG	Curt Blanding	1-10-79	
	Z Liggett	1/10/79	
APPD	Shannon Penn	1/10/79	

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DASH NO.	PART NO.	REV
10	0112-0130	B
	0112-0130	B

K100 — SHEET 1 of 1

Figure 7.4 K100-D/32 Input Adapter Assembly 0112-0130

ITEM	QUANTITY PER ASSEMBLY .60	.50	.40	.30	.20	TY.	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1						1	0112-0137	PWB				
2						A/R	———	BUSS WIRE			24 GA.	
3						1	1800-0296	I.C.	1B	OCTAL BUFFER	74S241 J	*
4						1	1800-0295	IC	1A	OCTAL INVERTER	74S240 J	*
5						1	1800-0038	IC	1C	DUAL 4-IN NAND	74S20	
6						1	1850-0006		2D	DUAL D FLIP-FLOP	10131	
7						1	1850-0048		2C	HEX BUFFER	10195	
8						1	1850-0003		3D	TRIPLE GATE, NOR	10105	
9						4	1800-0240		2,3,4,5A	OCTAL BUFFER	74LS244	
10						4	1800-0297		2,3,4,5B	OCTAL REGISTER	74S374J	*
11						4	1850-0021	I.C.	4C,5C,4D,5D	QUAD TTL→ECL	10124	
12						4	3000-2200	RESISTOR	R2,3,16,18,		220Ω 1/4W 5%	
13						4	3000-1500	RESISTOR	R6,14,17,23		150Ω 1/4W 5%	
14						2	3000-3300		R5,15		330Ω 1/4W 5%	
15						1	3000-3001		R11		3K 1/4W 5%	
16						2	3000-3006		R9,10		30Ω 1/4W 5%	
17						1	3000-7506		R21		75Ω 1/4W 5%	
18						3	3000-4700	RESISTOR	R19,20,22		470Ω 1/4W 5%	

REV	DESCRIPTION	ECO	DATE	APPROVED
A	PROTOTYPE			
B	CHANGE J1			
C	PILOT RELEASE EN0964			
D	REVISED PER ECO Nº 849		6-14-79	Ritter TM
E	REVISED PER ECO Nº 0856		7-16-79	Carroll TM
F	REVISED PER ECO Nº 0880		7-16-79	Carroll TM
G	REVISED PER ECO Nº 0929		9-21-79	Carroll TM

NANCY GAINES 6-13-78
T. McCann 1-9-79
Curt Blanding 1-10-79
1/9/79
1/10/79

-10 0112-0130 1
REF

LIST OF MATERIAL
P.W.B. ASSY
32 CHANNEL
ADAPTOR ASSEMBLY

bionation

B | 0112-0135 | L

K100D/32

PART 1 2

ITEM	QUANTITY PER ASSEMBLY .60	.50	.40	.30	.20	TY.	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
19						1	3000-7501	RESISTOR	R8		7.5K 1/4W 5%	
20						—	DELETED	———				
21						2	3300-0048	POT	R4,12		2K, 1T	
22						1	3700-0021	RESISTOR-PAK	RP1		470Ω 8-PIN SIP	
23						2	3000-1000	RESISTOR	R13,24		100Ω, 1/4W, 5%	
24						1	3000-8200	RESISTOR	R7		820Ω., 1/4W, 5%	
25						1	3000-1001	RESISTOR	R1		1K 1/4W, 5%	
26						1	6400-0041	L.E.D.	CR1		GREEN	
27						4	6100-0121	SOCKET	@2,3,4,5B		20 PIN	
28						13	4000-0025	CAPACITOR	C1-3, 7-16		.1 μf	
29						1	9000-0054	BUSS WIRE				
30						2	4100-0001	CAPACITOR	C4,5		100 pf	
31						2	4300-0025	CAPACITOR	C6,17		47/6V	
32						1	7200-0025	MOUSE TAIL				
33						1	0112-0131-10	CABLE ASSY.	J2 INPUT A (K,C,A,F,...,8		50 pin flat cable assy	LM
34						1	0112-0131-20	CABLE ASSY	J3 INPUT B (Z,A1,7,...,0		50 pin flat cable assy	LM
35						1	0010-0055	CABLE ASSY.			POWER CABLE, 10-TC .6 Ft. long	LM
36						2	1300-0007	TRANSISTOR	Q1, Q2		2N5179	

REV	DESCRIPTION	ECO	DATE	APPROVED
H	REVISED PER ECO Nº 0944		10-12-79	Carroll TM
J	REVISED PER ECO Nº 0970		10-23-79	Carroll TM
K	REVISED PER ECO 977		10-23-79	Carroll TM
L	REVISED PER ECO 1392		2-27-81	Burton JK

NANCY GAINES 6-13-78

LIST OF MATERIAL
P.W.B. ASSY
32 CHANNEL
ADAPTOR ASSEMBLY

bionation

B | 0112-0135 | L

REF

K100D/32

PART 2 2

Figure 7.5 K100-D/32 Input Adapter Assembly 0112-0135

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